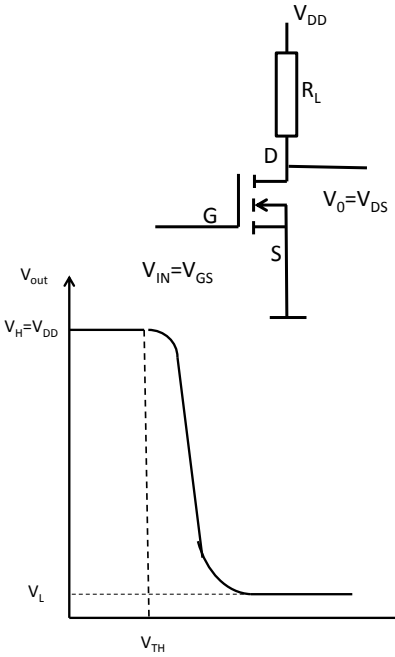
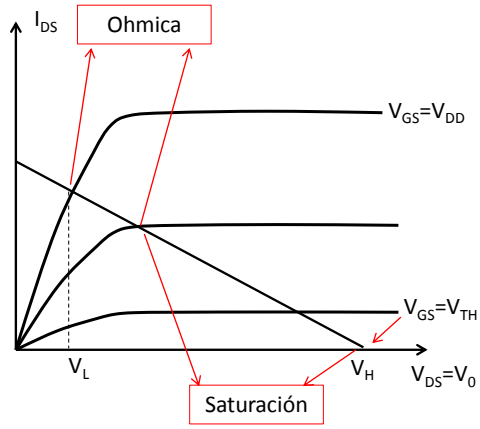
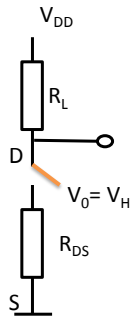
Inversor NMOS



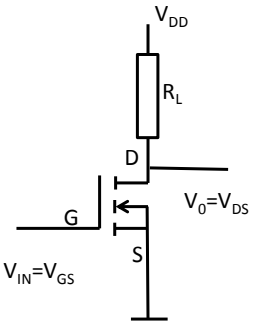


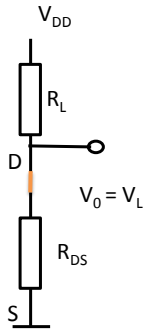
- Al variar V_{IN} desde 0 a V_{DD} el MOS pasa por:
  - I Zona de corte
  - II Zona de saturación
  - III Zona óhmica

Inversor NMOS



Salida en estado lógico alto

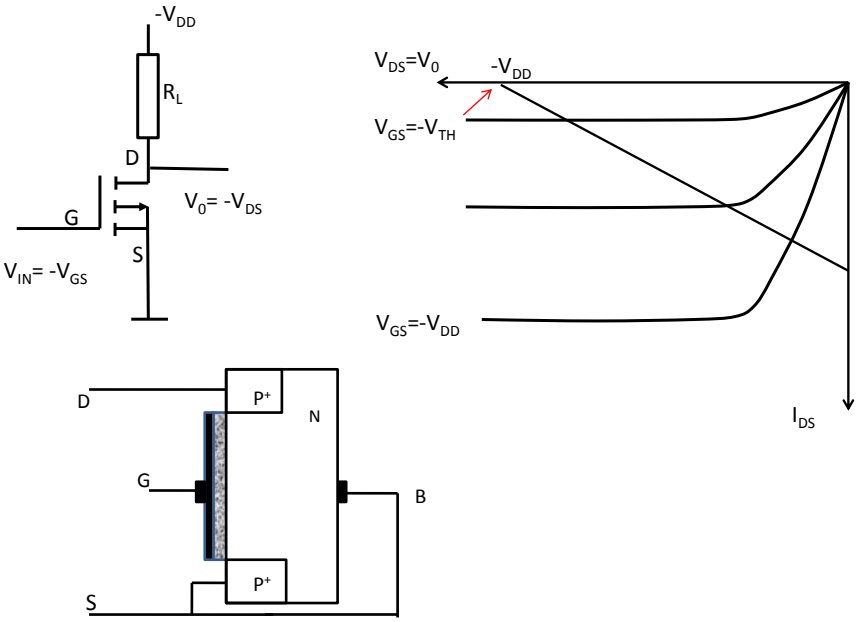




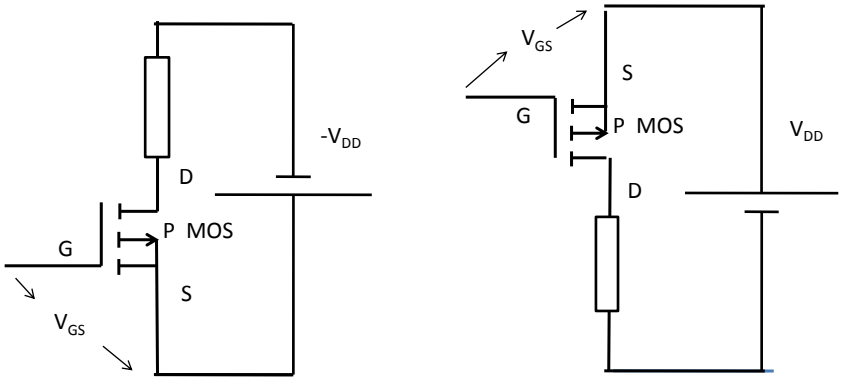
Salida en estado lógico bajo

$$P_E \approx \frac{1}{2}\frac{V_{DD}^2}{R_L}$$

Inversor PMOS

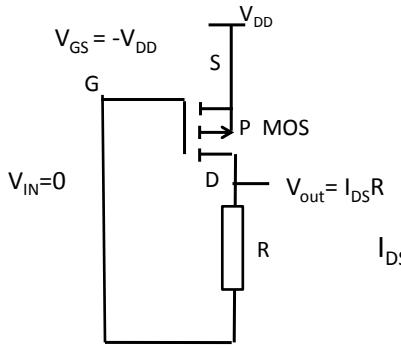


INVERSOR P MOS



INVERSOR P MOS

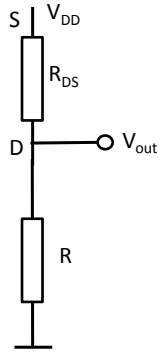
$V_{IN}=V_{DD}+V_{GS}$ $\quad V_{out} = I_{DS}R$



$|V_{TH}| < |V_{GS}|$

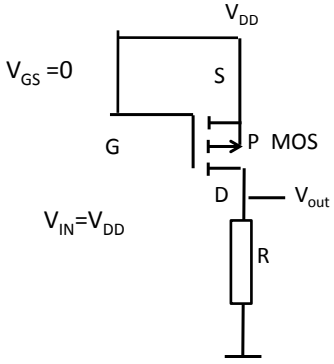
MOS → CONDUCE

I_{DS} Óhmico o Saturado



INVERSOR P MOS

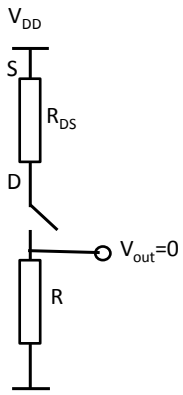
$V_{IN}=V_{DD}+V_{GS}$ $\quad V_{out} = 0$



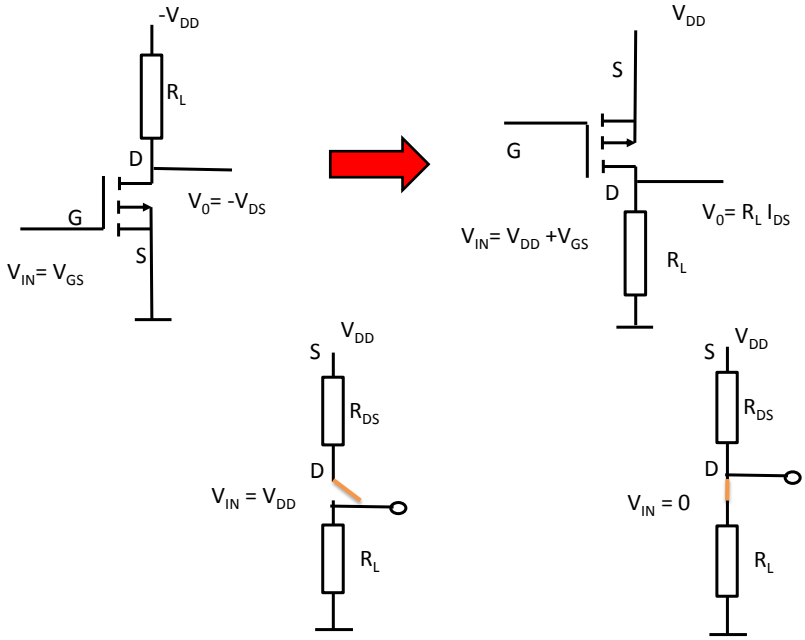
$|V_{TH}| > |V_{GS}|$

MOS → CORTADO

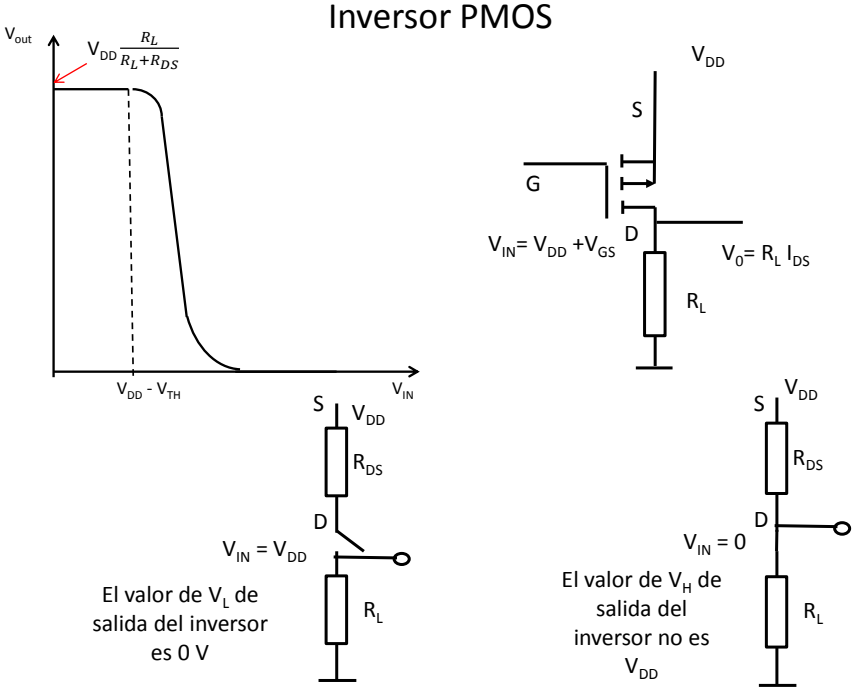
$V_{out} = 0$



Inversor PMOS



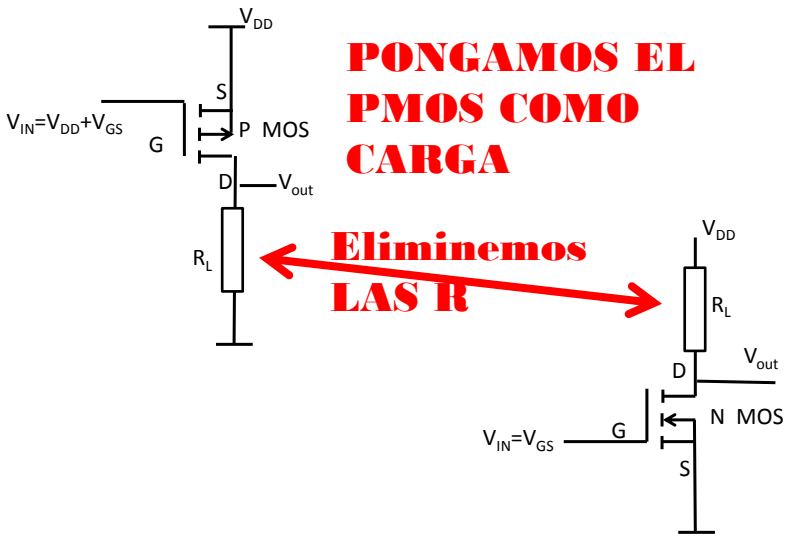
Inversor PMOS



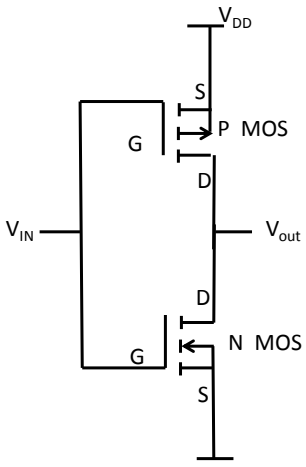
El valor de V_L de salida del inversor es 0 V

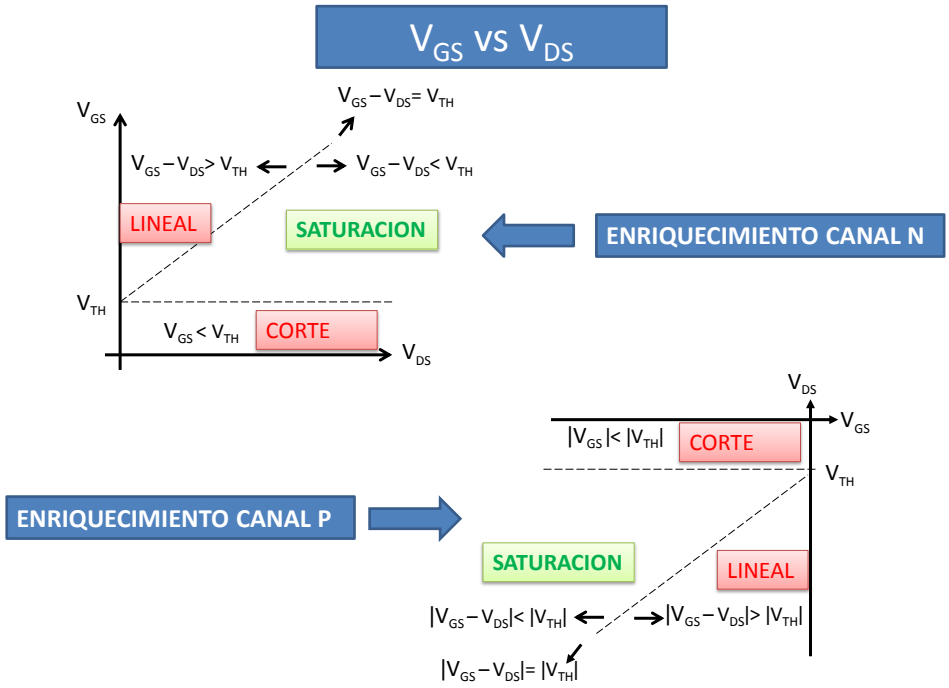
El valor de V_H de salida del inversor no es V_{DD}

INVERSOR CMOS

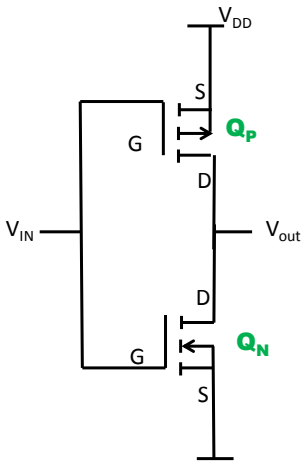


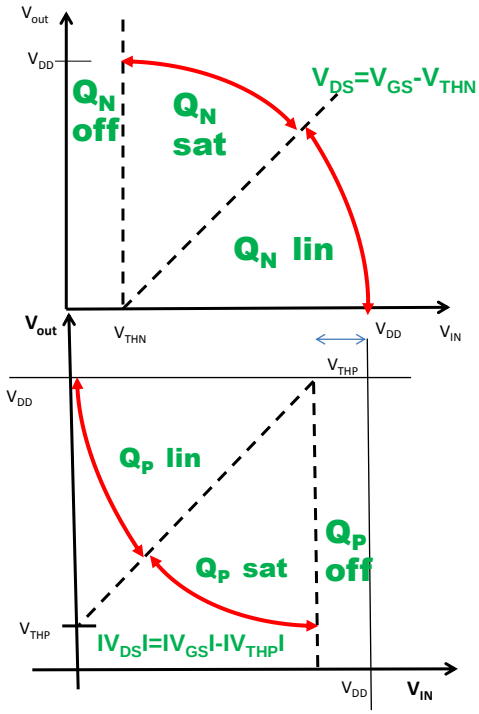
INVERSOR C MOS



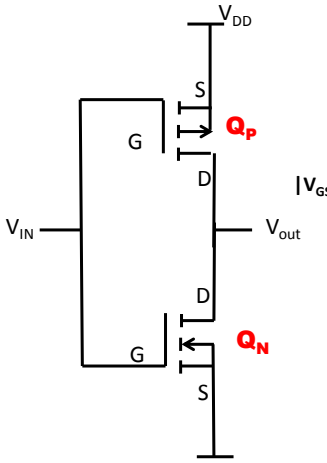


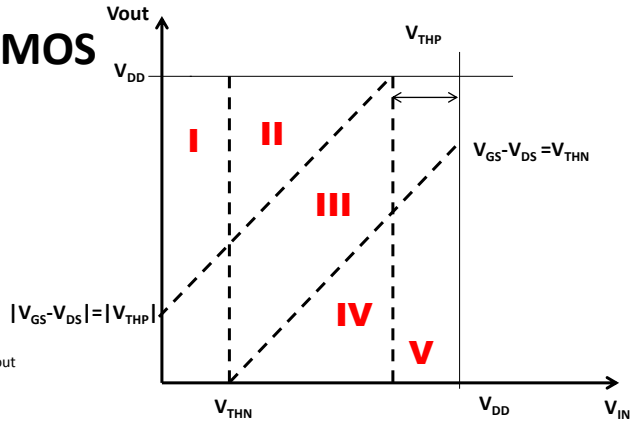
INVERSOR C MOS





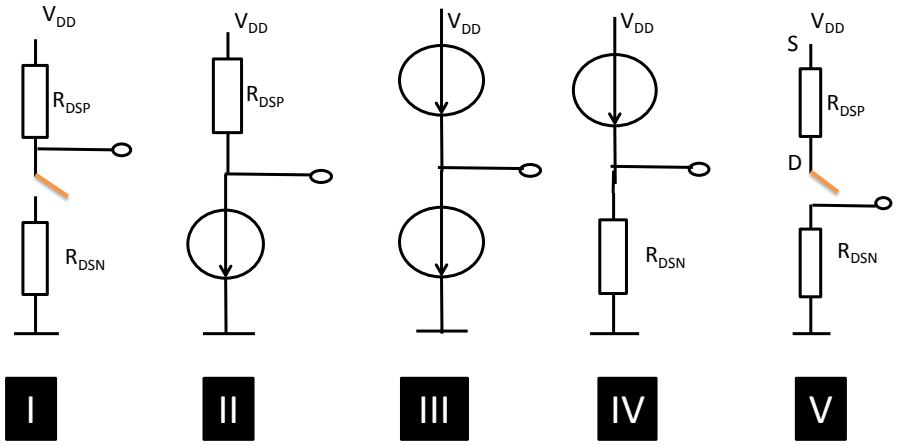
INVERSOR C MOS



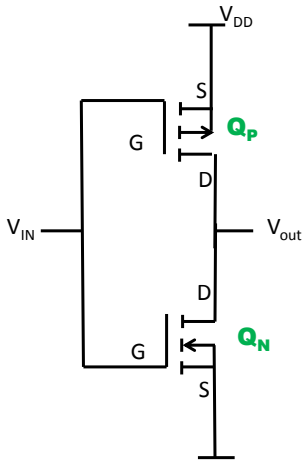


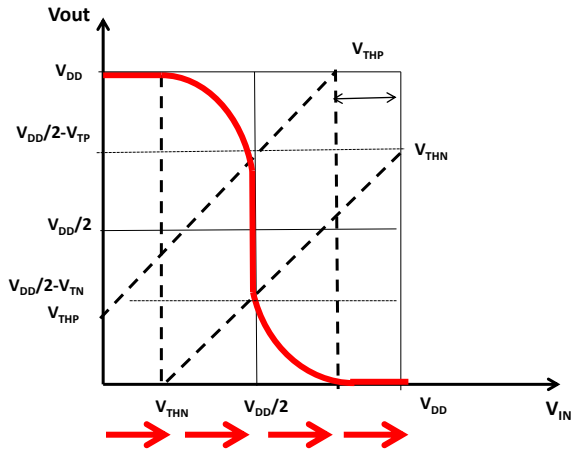
	Q_N	Q_P
I	off	lineal
II	satur	lineal
III	satur	satur
IV	lineal	satur
V	lineal	off

MODELOS SEGÚN ZONA DE OPERACION

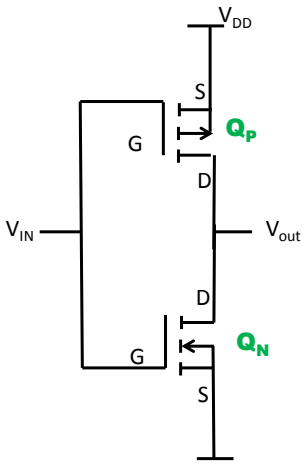


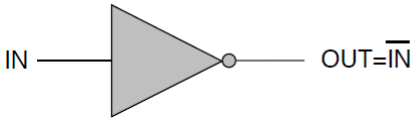
INVERSOR CMOS



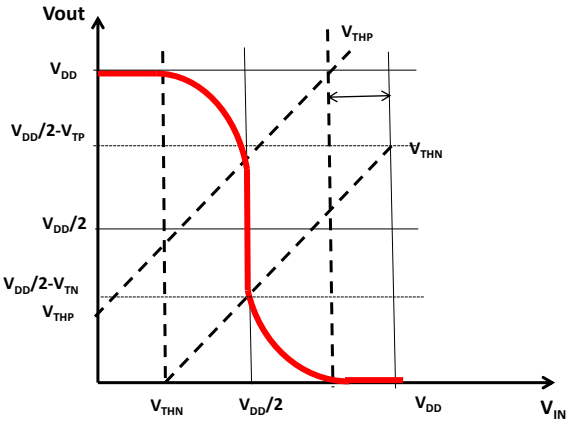


INVERSOR CMOS



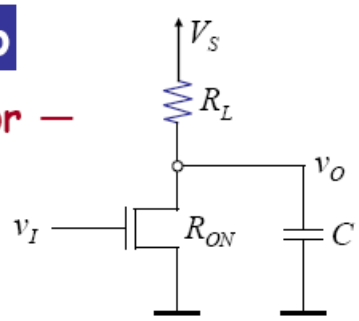


IN	OUT
0	1
1	0



Repaso

Inversor —



Entrada de onda cuadrada $T = \frac{1}{f}$

$$\overline{P} = \frac{V_S^2}{2R_L} + CV_S^2 f$$

$\overline{P}_{ESTÁTICO}$ — independiente de f. el MOSFET está ON la mitad del tiempo.

$\overline{P}_{DINÁMICO}$ — relacionado con el condensador de conmutación.

$R_L >> R_{ON}$

$\frac{T}{2} >>$ "RC" *constante de tiempo*

Algunos números...

Un chip con 10^6 puertas cronometrando a 100 MHZ

$C = 1f\,F$
$R_L = 10\,k\Omega$
$f = 100 \times 10^6$
$V_S = 5V$

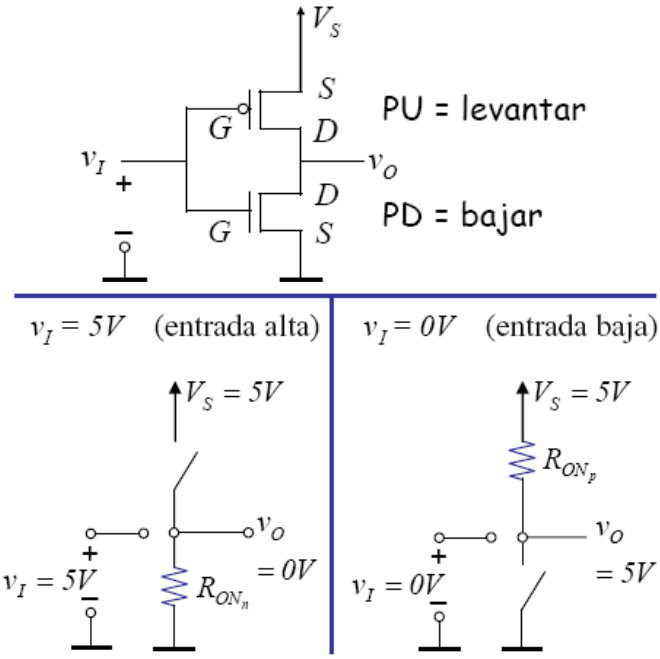
$$\overline{P} = 10^6 \left[\frac{25}{2 \times 10^4} + 10^{-15} \times 25 \times 100 \times 10^6 \right]$$

$$= 10^6 \left[1.25\ milivatios + 2.5\ microvatios \right]$$

¡problema! $1.25KW!$ debe deshacerse de esto

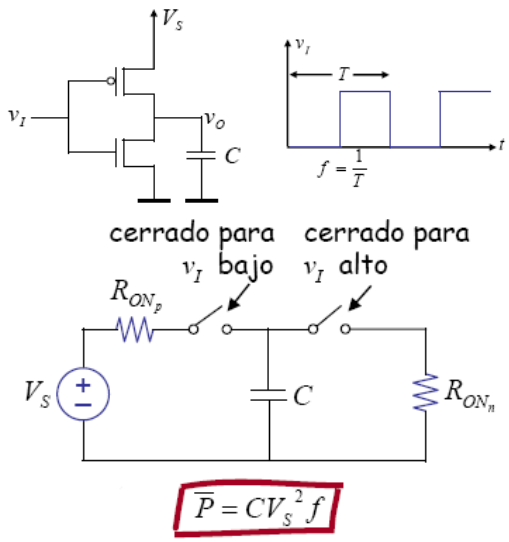
$2.5W$ no está mal

$\alpha\, V_S^2$
$\alpha\, f$
reduzca V_S
$5V \rightarrow 1V$
$2.5W \rightarrow 150\,mW$



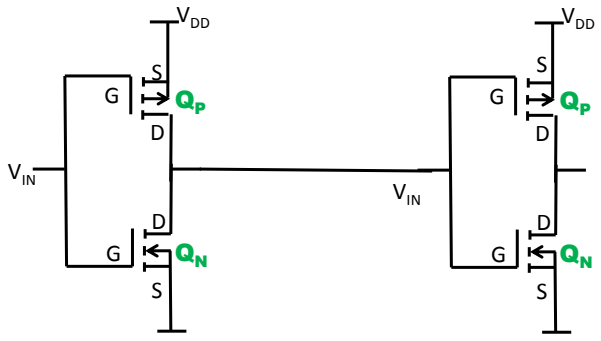
Clave: no hay camino desde V_S a GND
no hay potencia estática

Calculemos $\overline{P}_{DINÁMICO}$



$$\overline{P} = CV_S^2 f$$

INVERSOR C MOS



La disipación de Potencia será $P_{disipadaporciclo} = C_L V_{DD}^{\ 2} f$

Para nuestro ejemplo anterior—

$$C = 1fF,\ V_S = 5V,\ f = 100MHz,\ 1$$

$$\overline{P} = CV_s^{\ 2} f$$

$$= 10^{-15} \times 5^2 \times 100 \times 10^6$$

$$= 2.5\ \mu\text{vatios por puerta}$$

$$\overline{P} = 2.5\ \mu\text{vatios para el chip de puerta } 10^6$$

Puertas	f	$\overline{P}$	
10^6	100 MHz	~2.5 vatios	¿Pentium?
2×10^6	300 MHz	~15 vatios	¿PII?
2×10^6	600 MHz	~30 vatios	¿PII?
8×10^6	1.2 GHz	~240 vatios	¿PIII?
25×10^6	3 GHz	~1875 vatios	¿PIV?

"deje todo lo demás igual"

Cómo reducir potencia

Ⓐ V_S 5V → 3V → 1.8V → 1.5V
~PIV → 170 vatios → mejor, pero alto

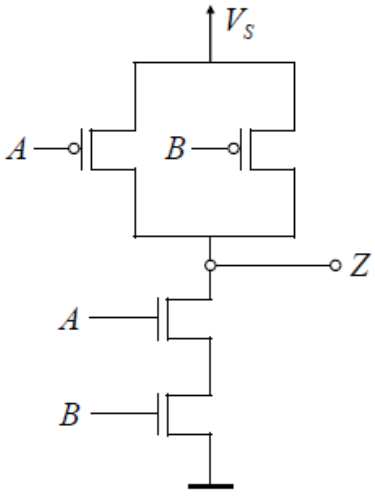
y utilice un disipador de calor grande

Ⓑ Desconecte el reloj cuando no se esté utilizando.

Ⓒ Cambie V_S según las necesidades.

LOGICA CMOS

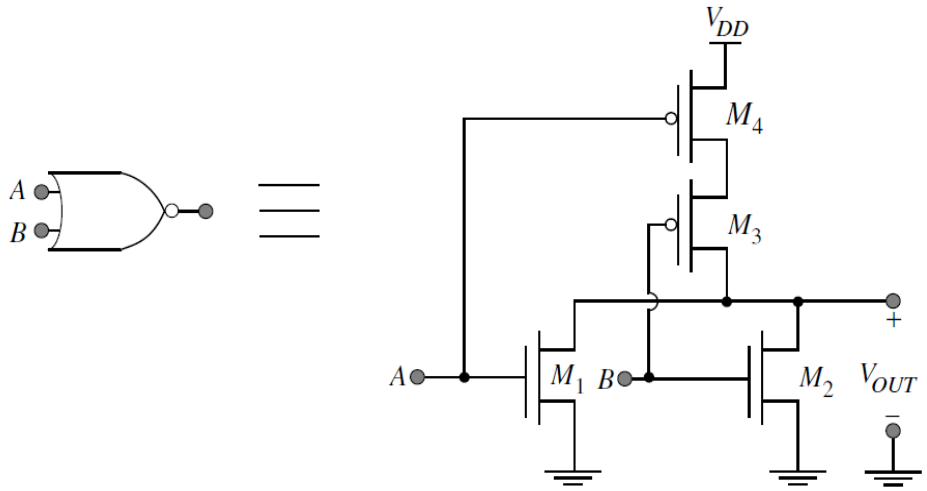
COMPUERTA NAND



A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

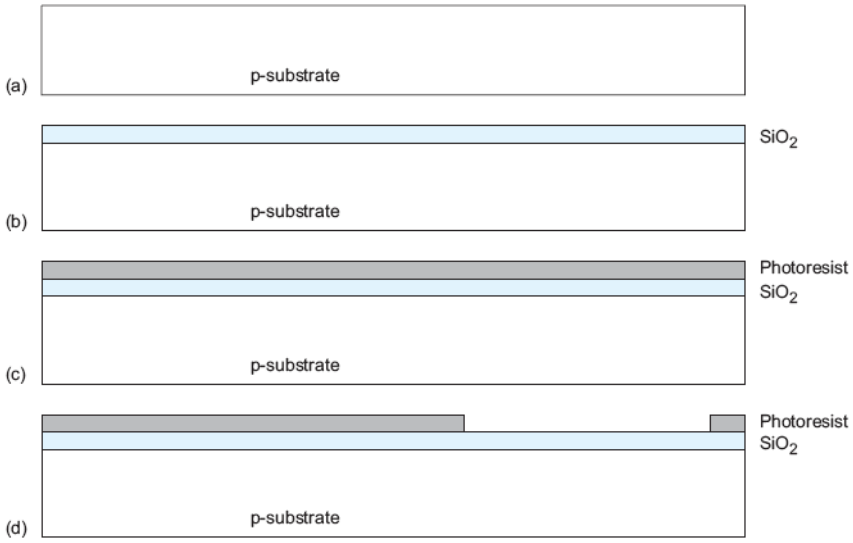
LOGICA CMOS

COMPUERTA NOR

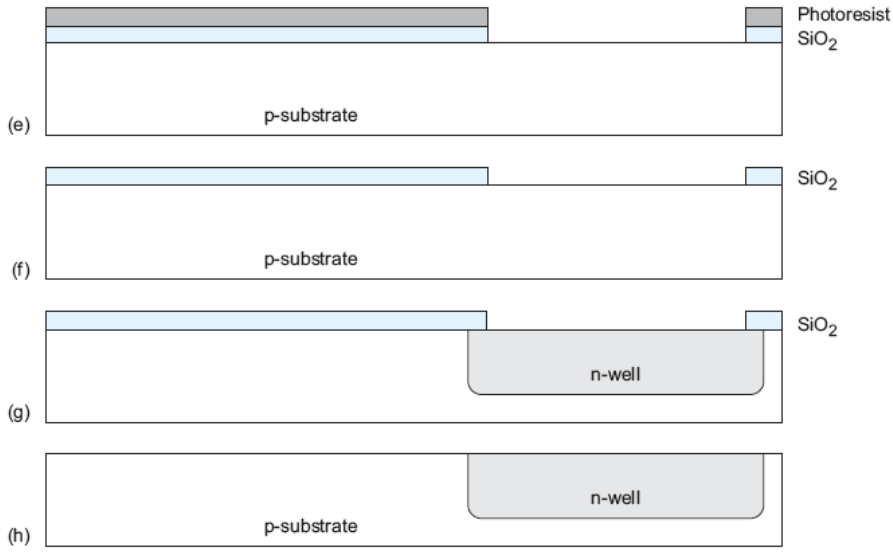


Fabricación de un inversor CMOS

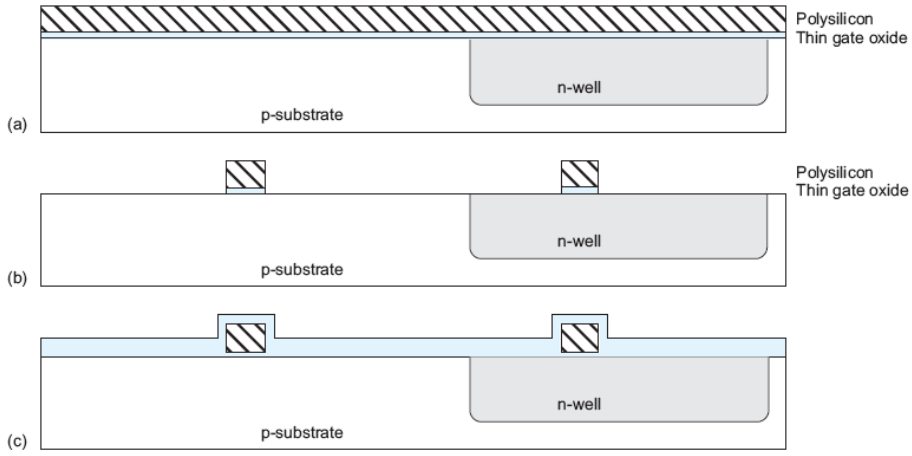
I



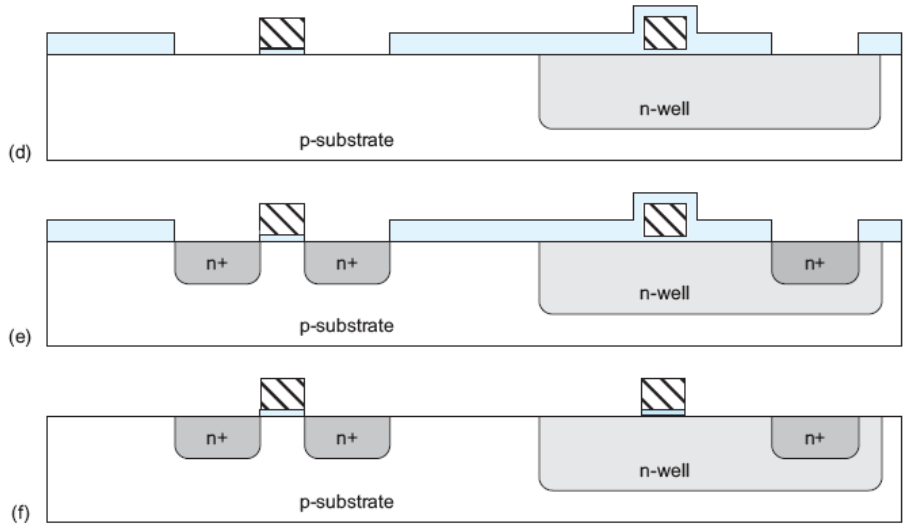
Fabricación de un inversor CMOS II



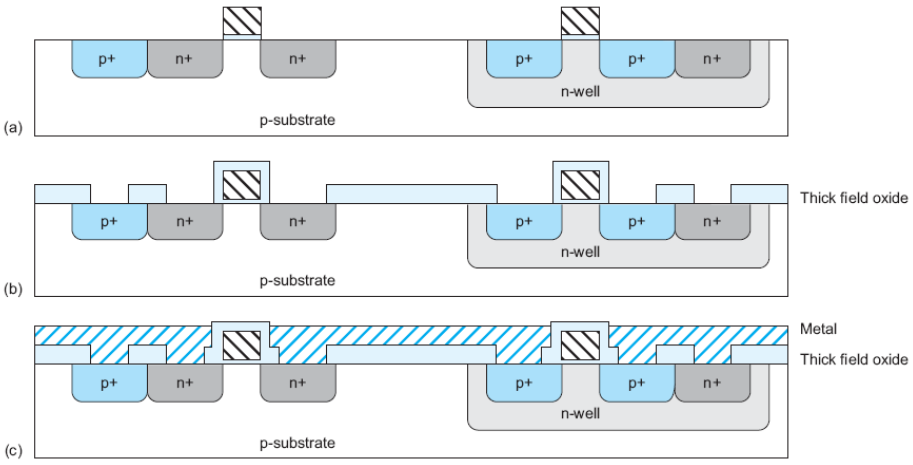
Fabricación de un inversor CMOS III



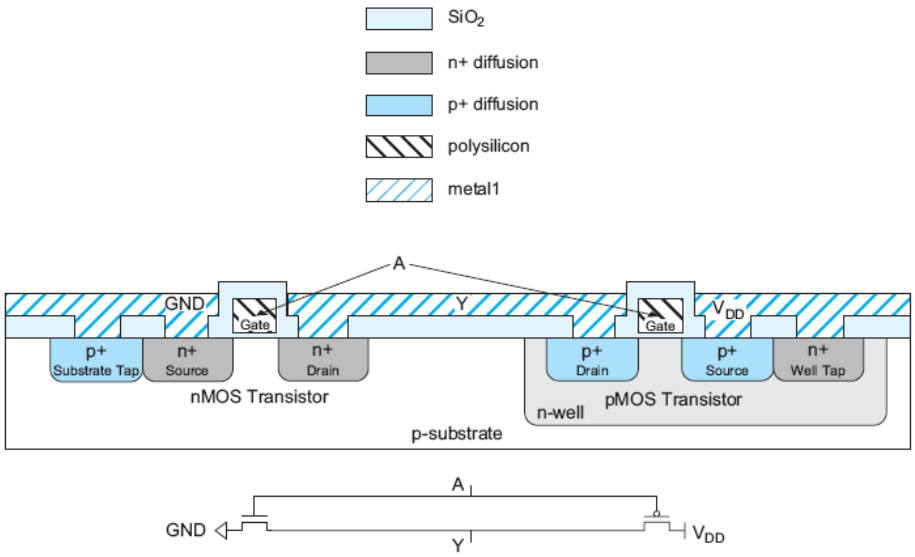
Fabricación de un inversor CMOS

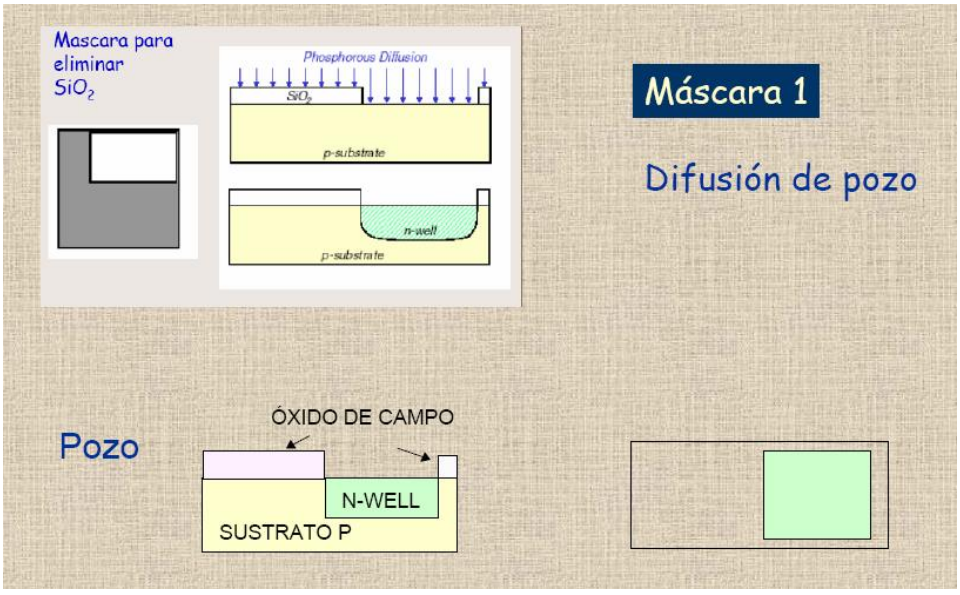


Fabricación de un inversor CMOS
IV

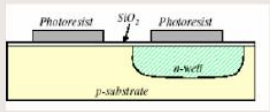


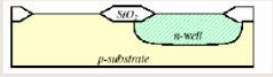
Corte transversal de un inversor CMOS





Define las regiones activas donde se van a colocar los dispositivos

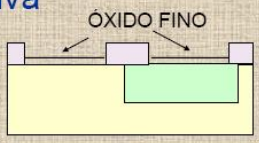


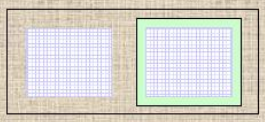


Máscara 2

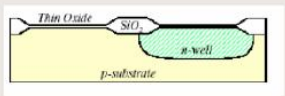
Definición de áreas activas

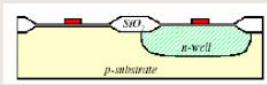
Área activa





Se deposita el polisilicio de puerta

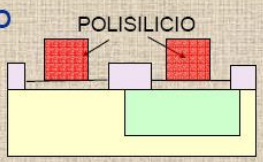


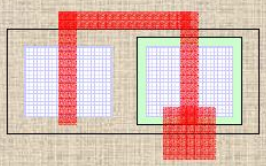


Máscara 3

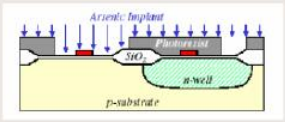
Definición de las puertas

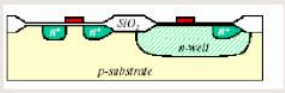
Polisilicio





Se crea la fuente y el drenador de los dispositivos n

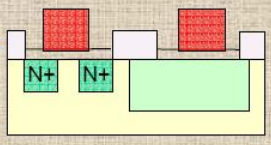


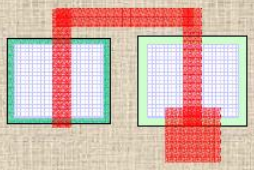


Máscara 4

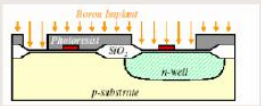
Difusión n+
MOS canal N

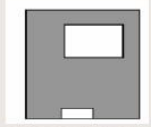
Implante N+

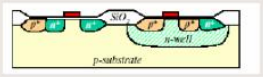




Se crea la fuente y el drenador de los dispositivos p



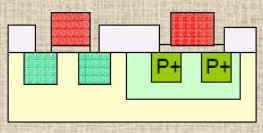


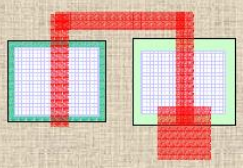


Máscara 5

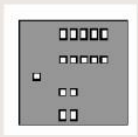
Difusión p+
MOS canal P

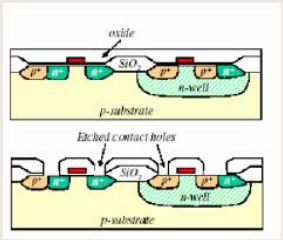
Implante P+





Determina las posiciones donde van los contactos

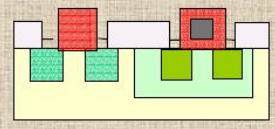


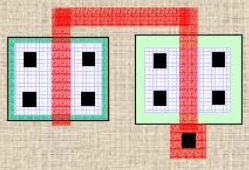


Máscara 6

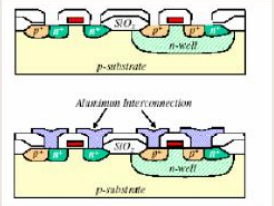
Perforaciones de contacto

Contactos





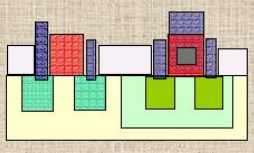
Determina las posiciones donde van las interconexiones

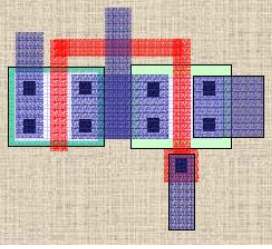


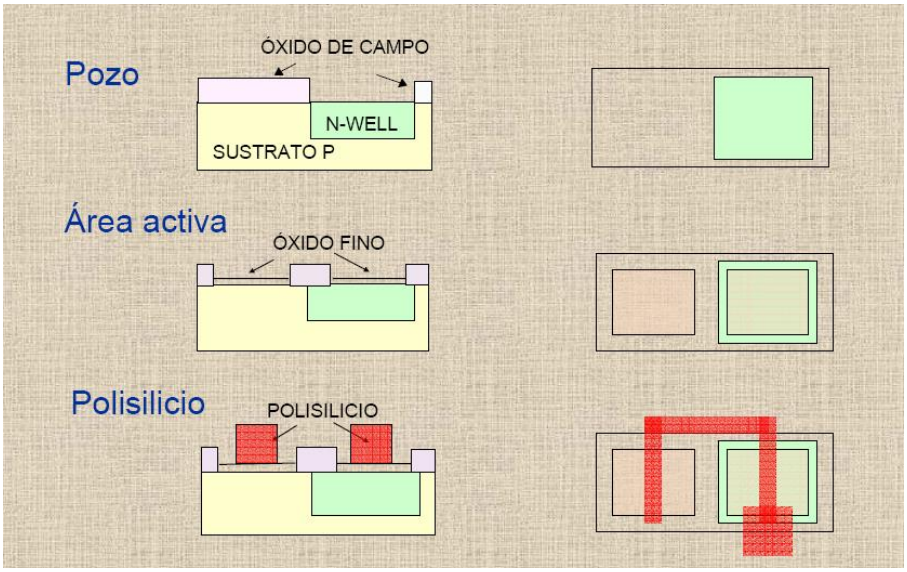
Máscara 7

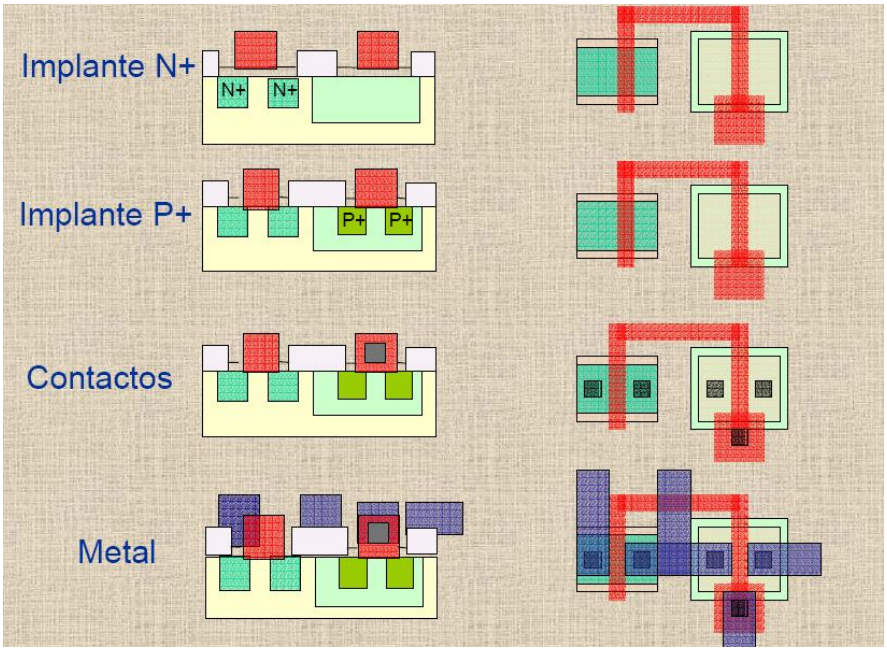
Metalización

Metal






Pozo
ÓXIDO DE CAMPO
N-WELL
SUSTRATO P
Área activa
ÓXIDO FINO
Polisilicio
POLISILICIO


Implante N+
N+
N+
Implante P+
P+
P+
Contactos
Metal