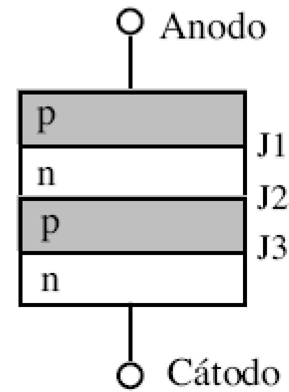
SCR DISPOSITIVO ELECTRONICOS

DIODO de 4 CAPAS

Definición Cualitativa

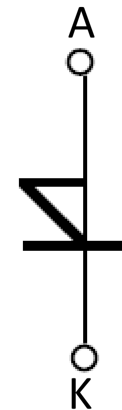
- **Dispositivo Semiconductor de 4 capas cuya estructura es PNPN**



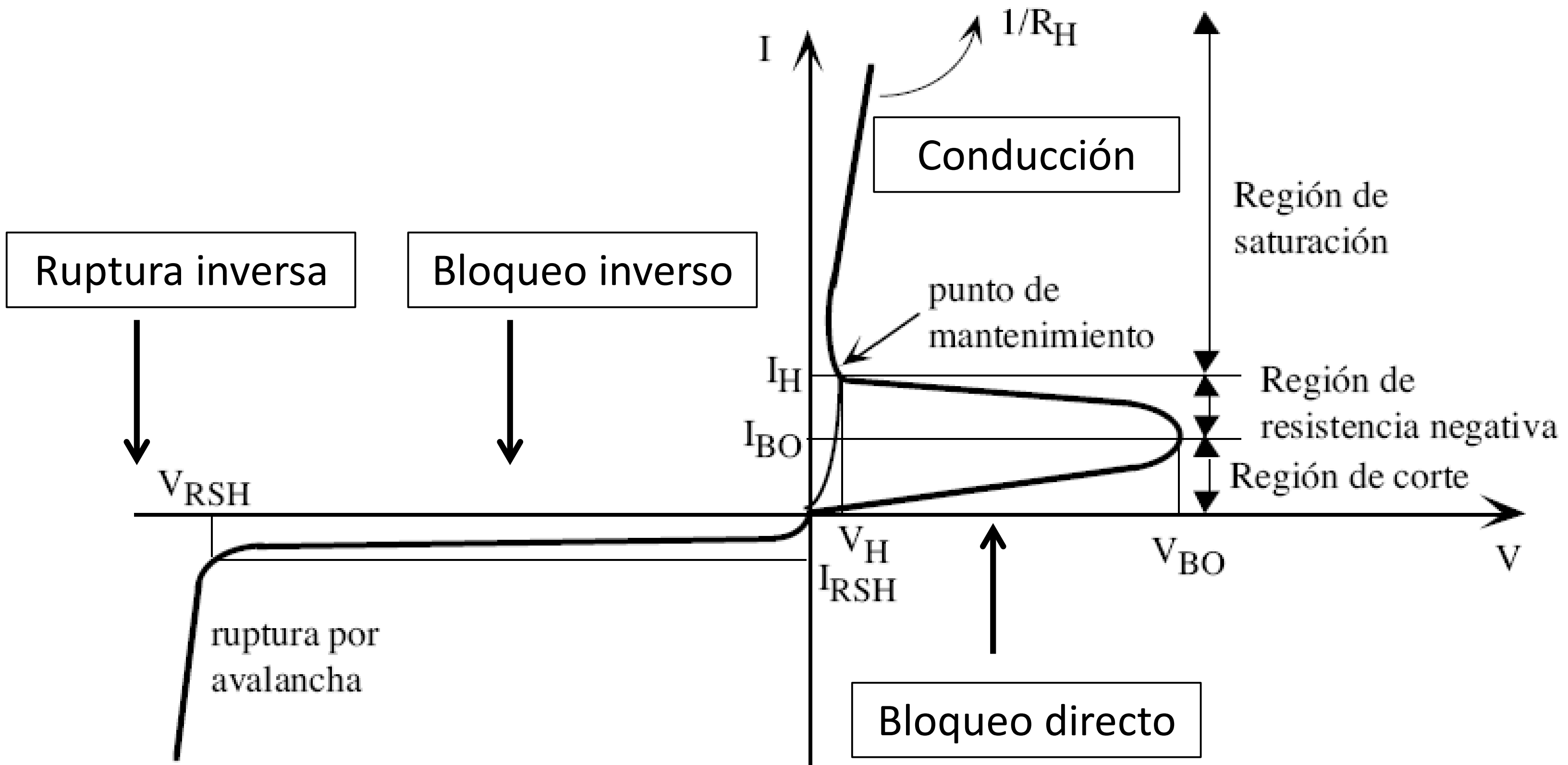
- **Tiene dos terminales Ánodo y Cátodo**

- **Función en el circuito: llave accionada por tensión**

- **Símbolo que lo representa en los Circuitos**

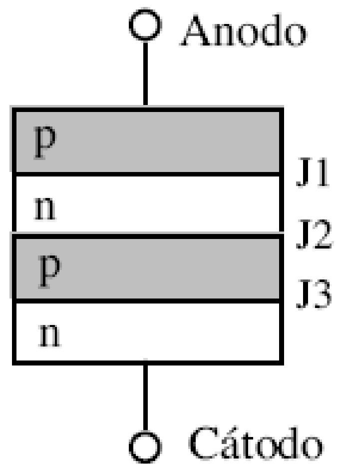


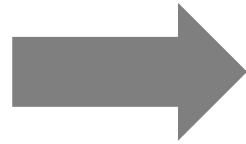
Características V-I

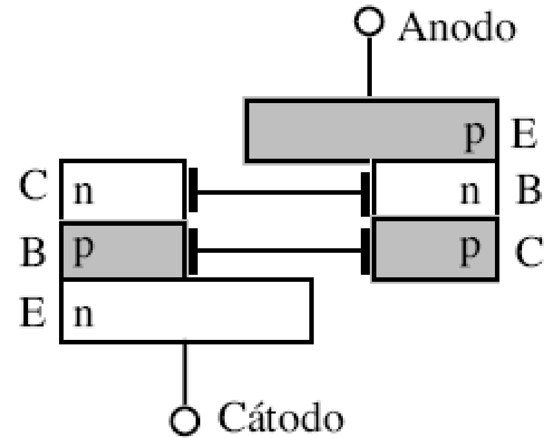


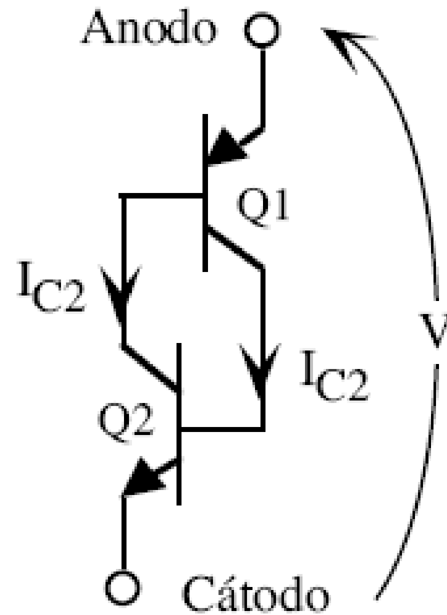
FUNCIONAMIENTO

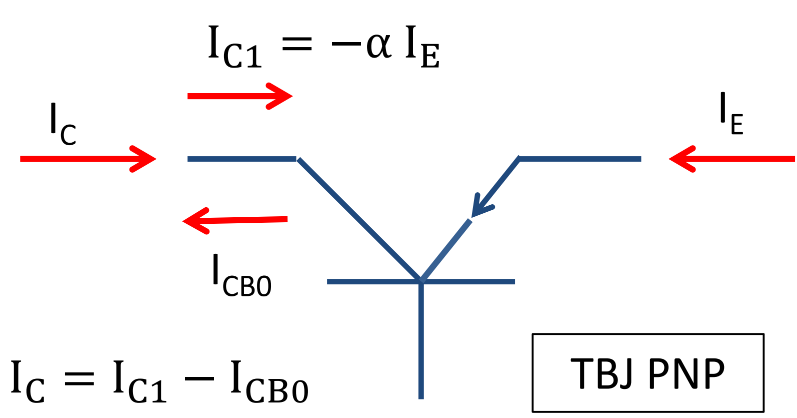
Modelo del DIODO de 4 Capas

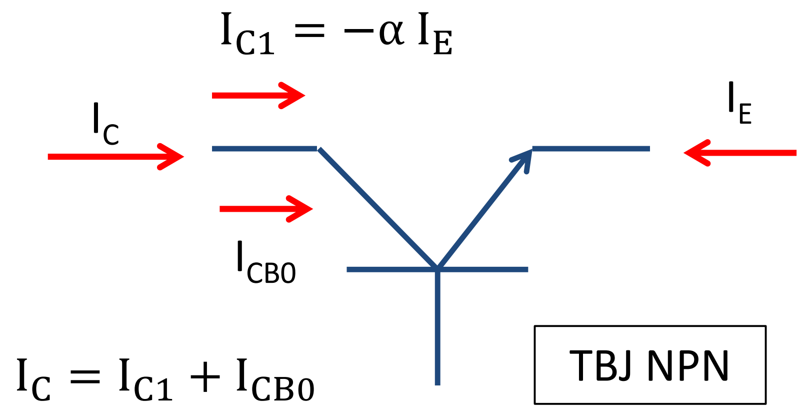












$$I_C = I_{C1} - I_{CB0}$$

$$I_C = -\alpha\, I_E - I_{CB0}$$

$$I_C = I_{C1} + I_{CB0}$$

$$I_C = -\alpha\, I_E + I_{CB0}$$

I_A Q1 I_{C2} I_{C1} Q2 I_A

$$I_A = I_{E1}$$

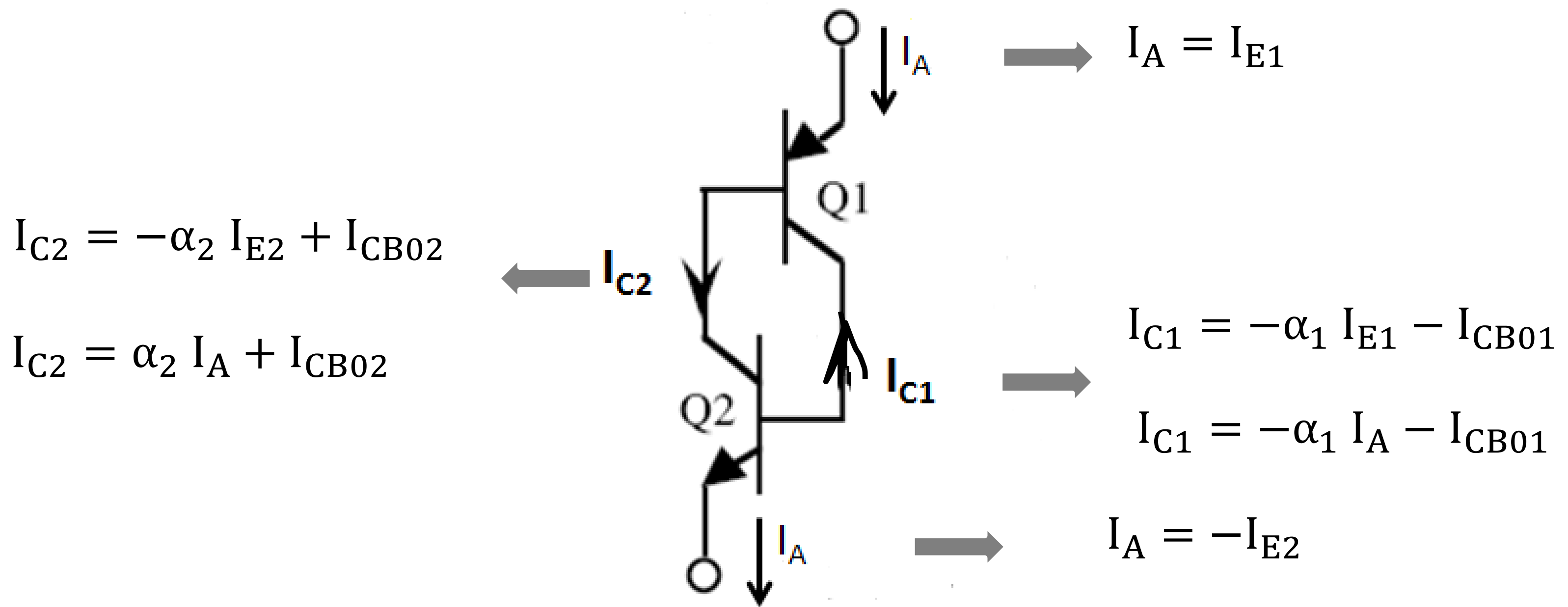
$$I_{C1} = -\alpha_1\, I_{E1} - I_{CB01}$$

$$I_{C1} = -\alpha_1\, I_A - I_{CB01}$$

$$I_A = -I_{E2}$$

$$I_{C2} = -\alpha_2\, I_{E2} + I_{CB02}$$

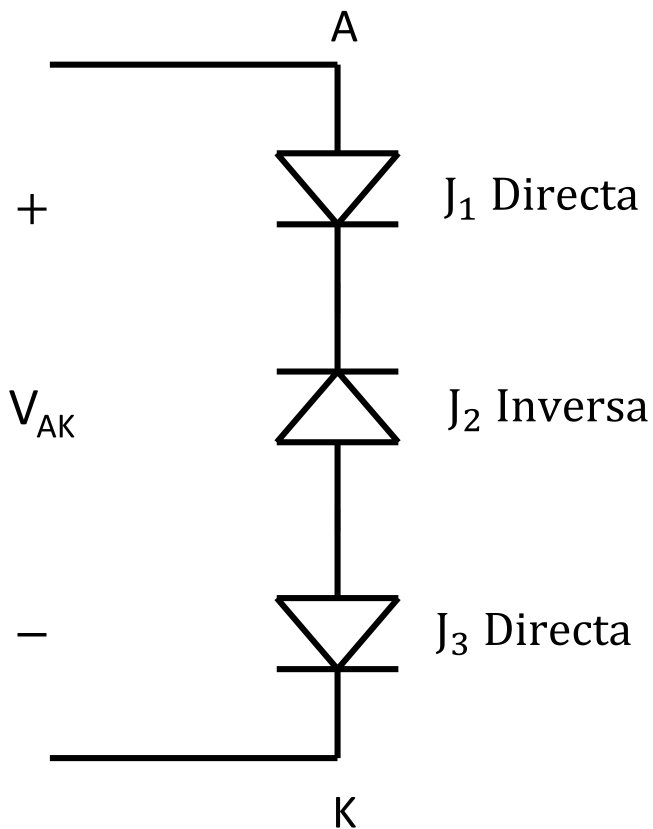
$$I_{C2} = \alpha_2\, I_A + I_{CB02}$$

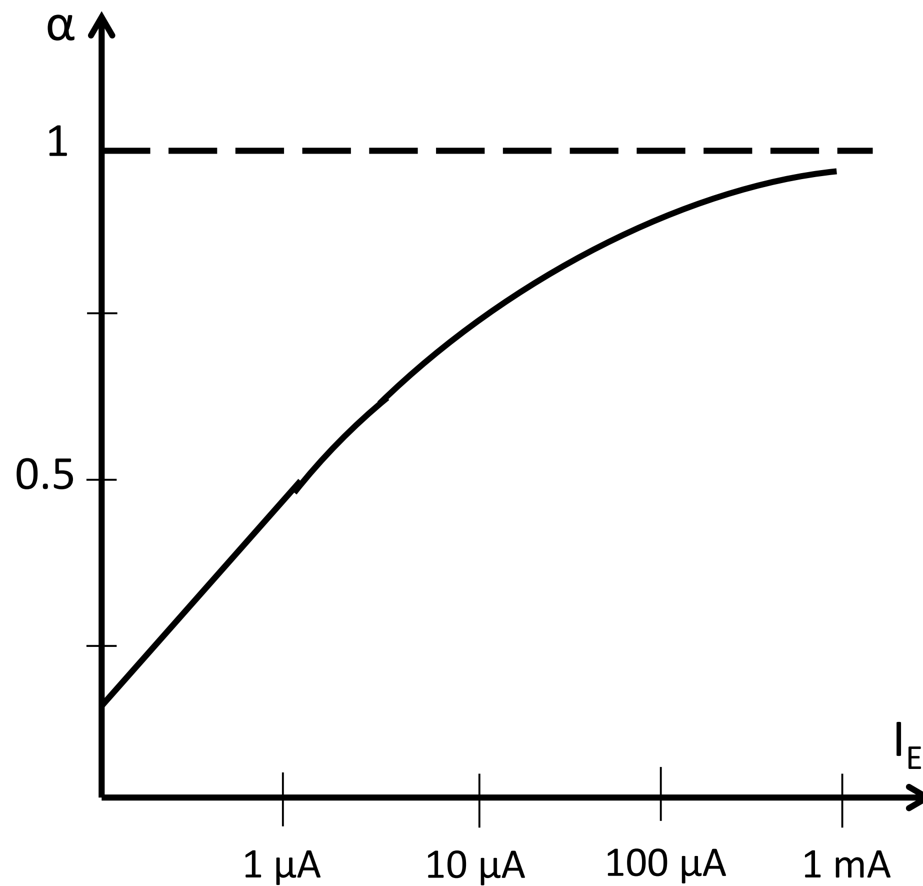


$$I_A + I_{C1} - I_{C2} = 0 \qquad I_A = I_{C2} - I_{C1} \qquad I_A = \alpha_2 \, I_A + I_{CB02} + \alpha_1 I_A + I_{CB01}$$

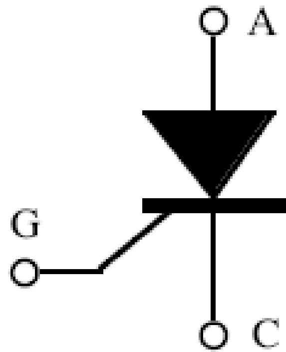
$$\boxed{I_A = \frac{I_{CBO1} + I_{CB02}}{1 - (\alpha_1 + \alpha_2)}}$$

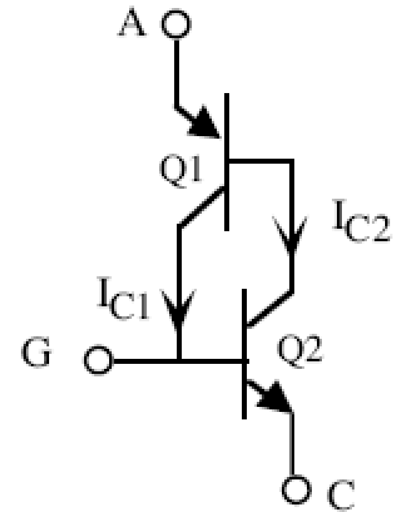
$$\boxed{\text{Si } (\alpha_1 + \alpha_2) = 1 \quad I_A \Longrightarrow \infty}$$

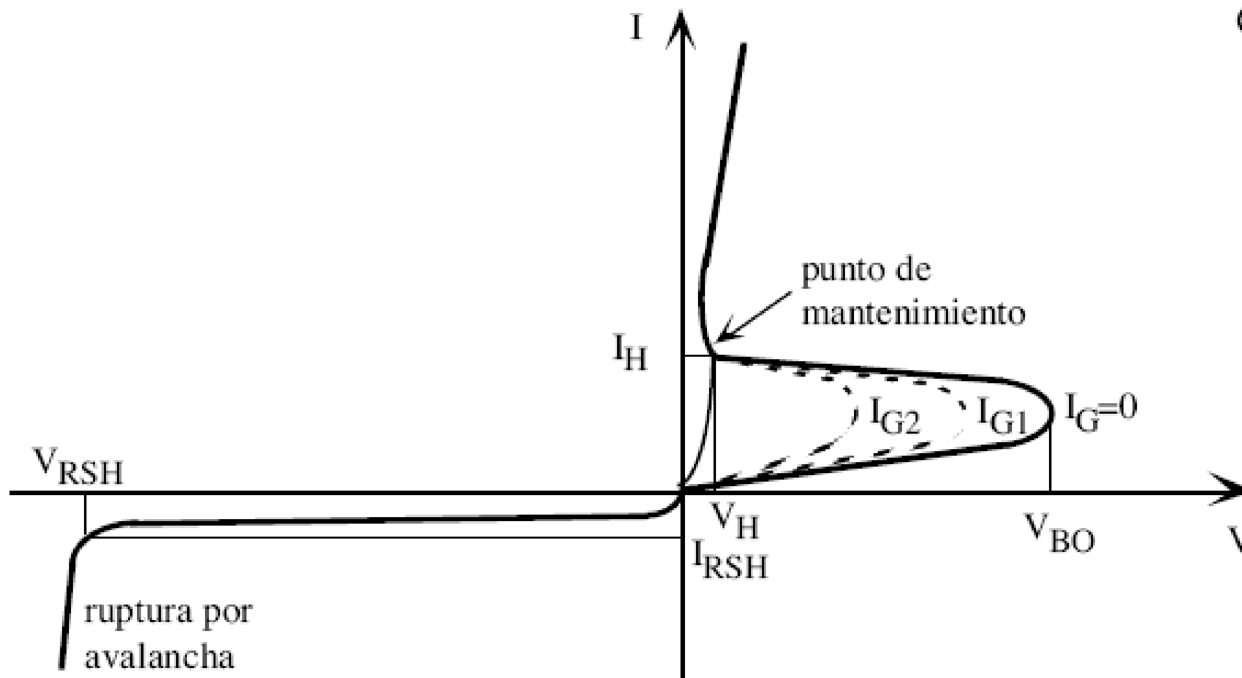

A
+
J1 Directa
VAK
J2 Inversa
−
J3 Directa
K


α
1
0.5
IE
1 μA
10 μA
100 μA
1 mA

Rectificador Controlado de Silicio SCR





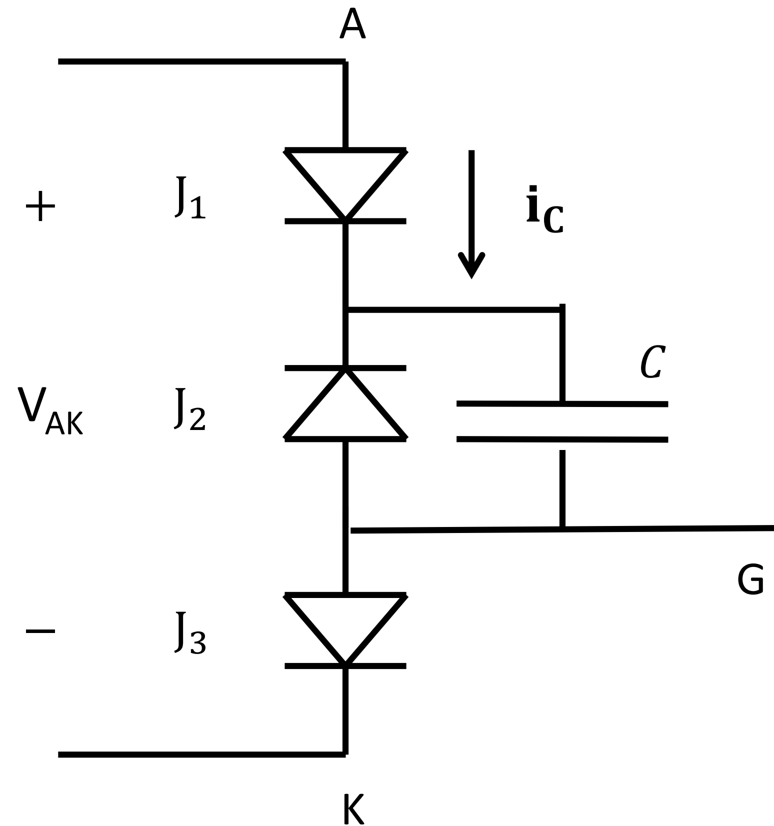


Limitaciones del Dispositivo

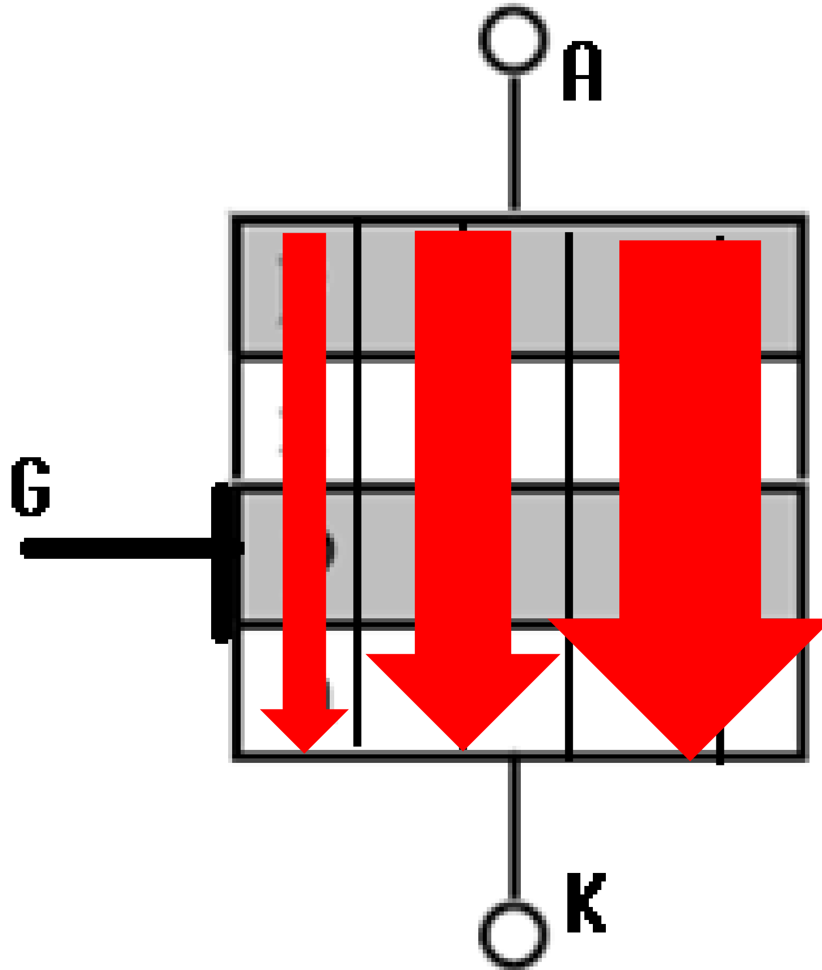
- Potencia Máxima V_{AK} x I_A

- $\frac{dV}{dt}$ **Máxima**

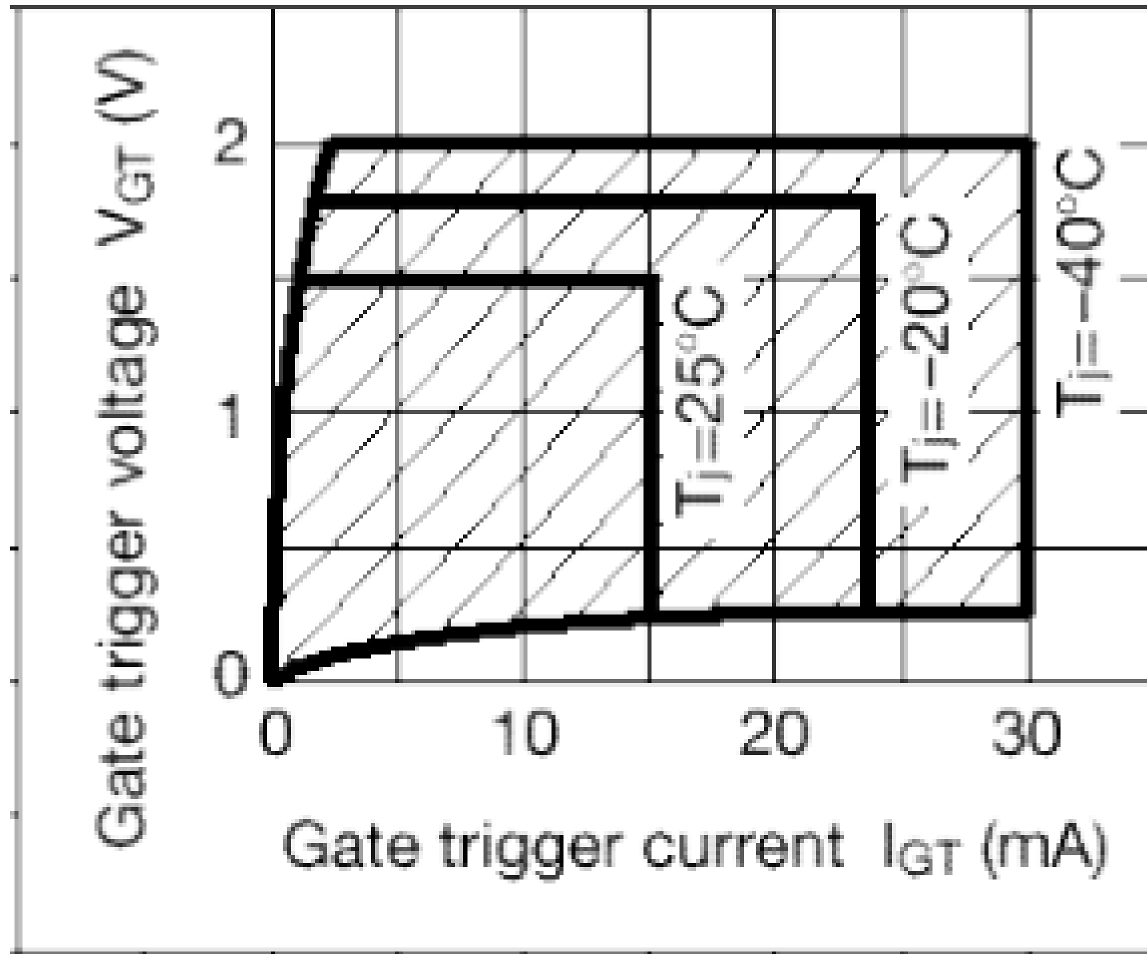
$$i_C = C\frac{dV}{dt}$$



- $\frac{dI}{dt}$ Máxima



ZONA DE DISPARO SEGURA



Thyristors BT145 series

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

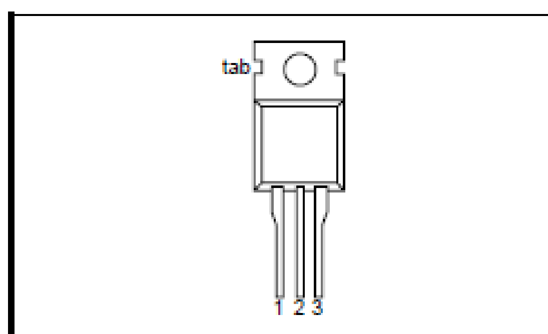
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT145-	500R	600R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	16	16	16	A
$I_{T(RMS)}$	RMS on-state current	25	25	25	A
I_{TSM}	Non-repetitive peak on-state current	300	300	300	A

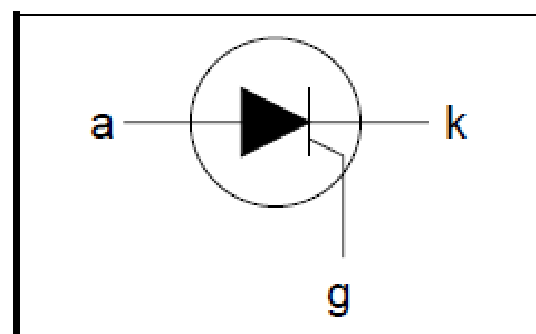
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 101$ °C	-	16			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	25			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25$ °C prior to surge					
		t = 10 ms	-	300			A
		t = 8.3 ms	-	330			A
I^2t	I^2t for fusing	t = 10 ms	-	450			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 50$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	200			A/µs
I_{GM}	Peak gate current		-	5			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	20			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			°C
T_j	Operating junction temperature		-	125			°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

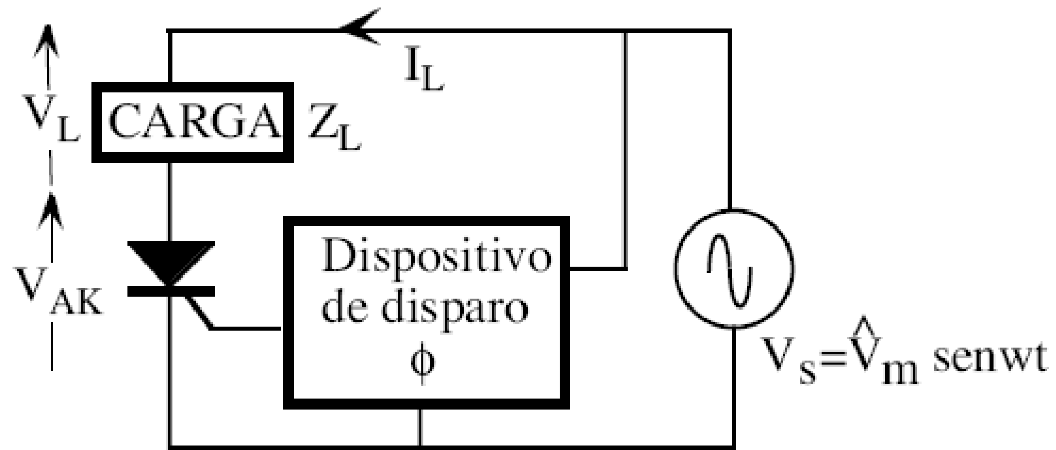
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	5	35	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	25	80	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	20	60	mA
V_T	On-state voltage	I_T = 30 A	-	1.1	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.0	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 °C	-	0.2	1.0	mA

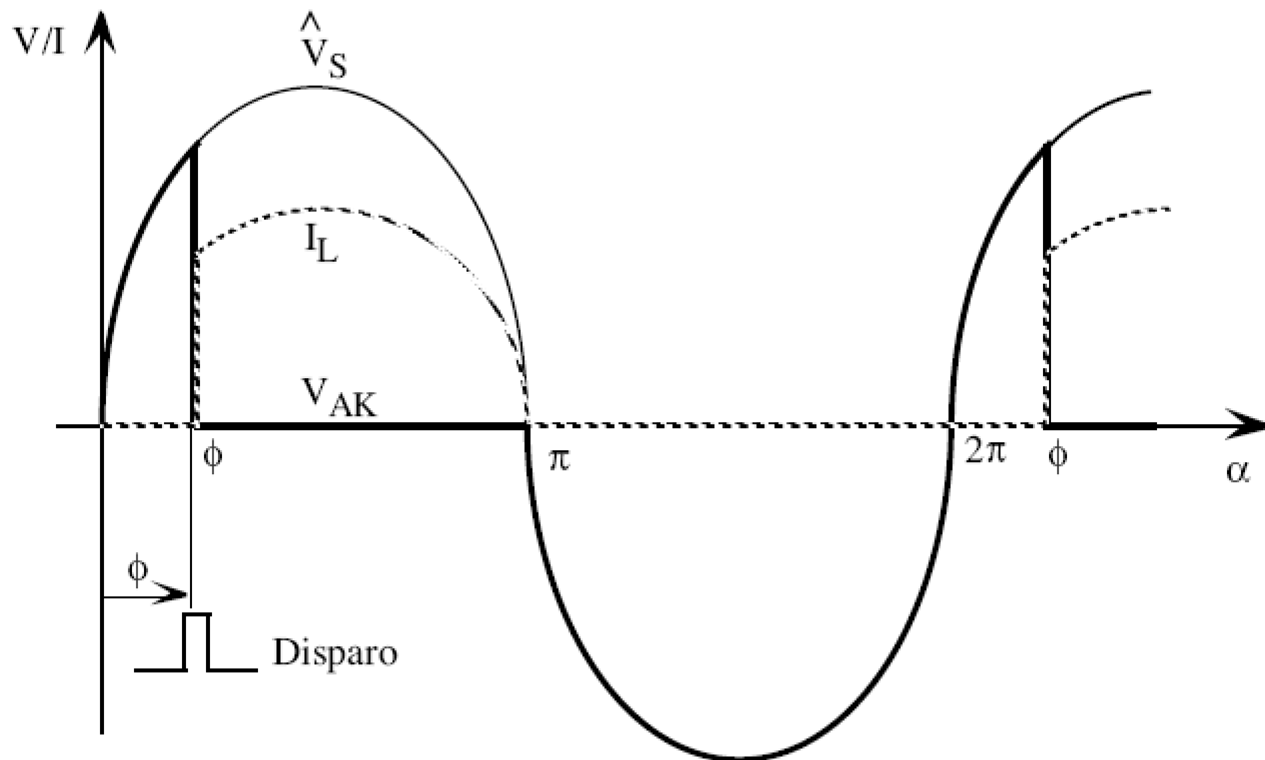
DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	200	500	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 °C; I_{TM} = 50 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs	-	70	-	µs

Regulación de potencia





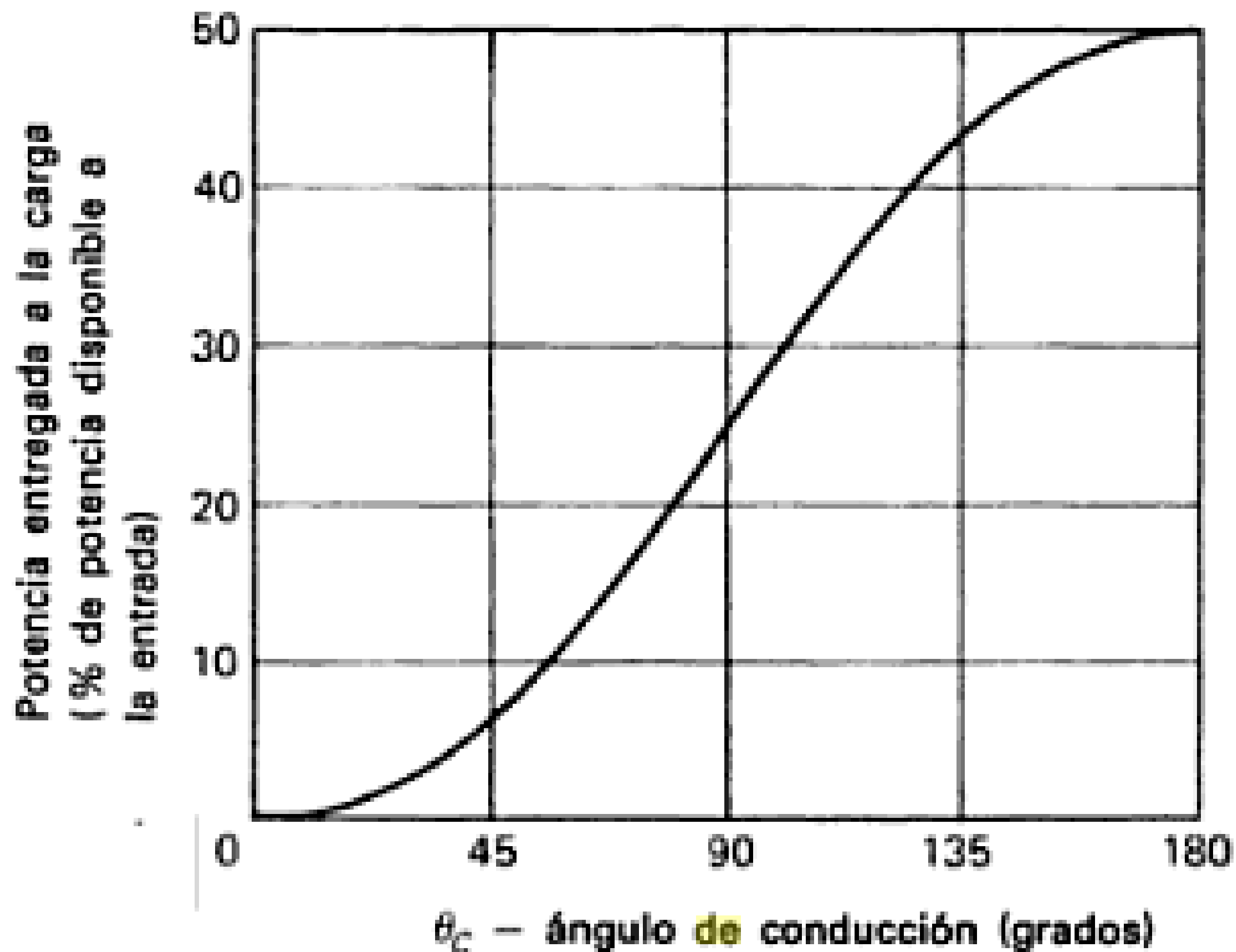
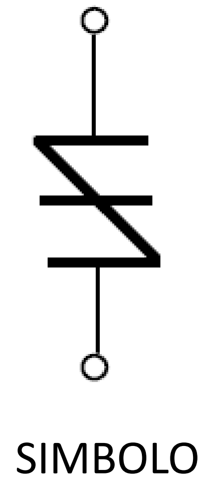


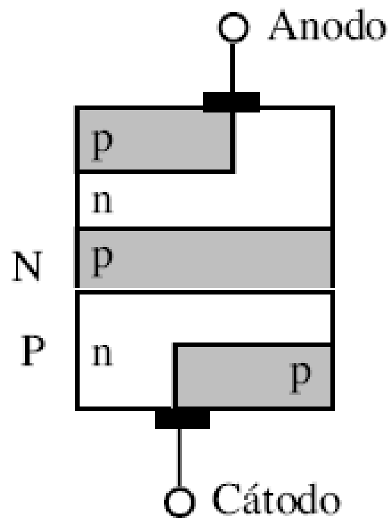
Fig. 20-6. Potencia entregada a la carga en función del ángulo de conducción, en un circuito de media onda.

SIDAC

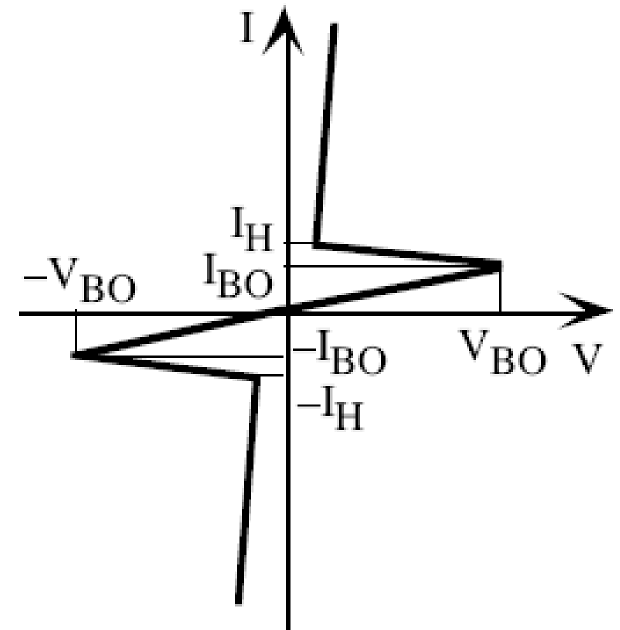
Diodo de 4 capas de características eléctricas simétricas



SIMBOLO

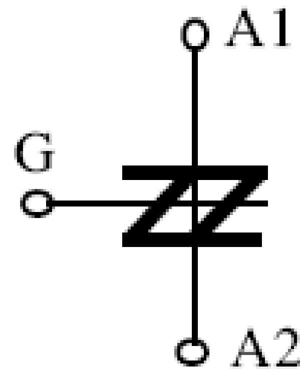


ESQUEMA CONSTRUCTIVO

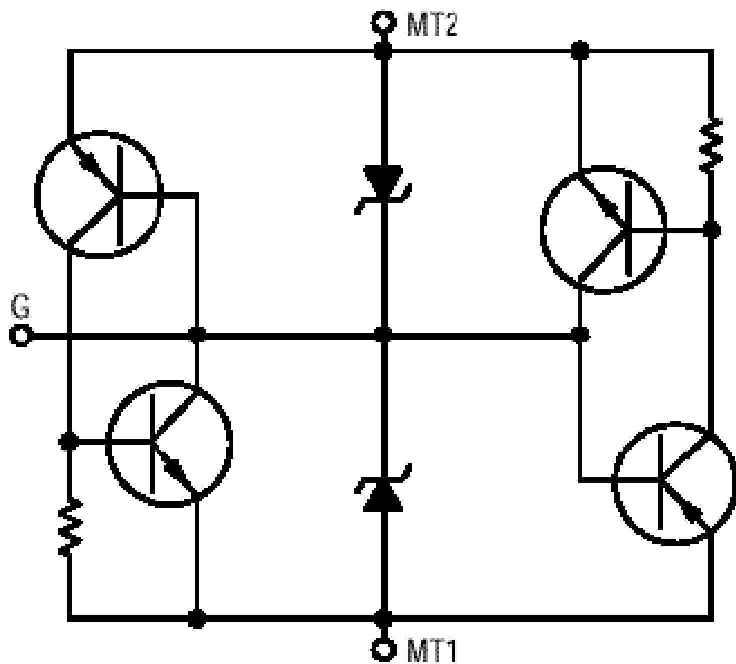


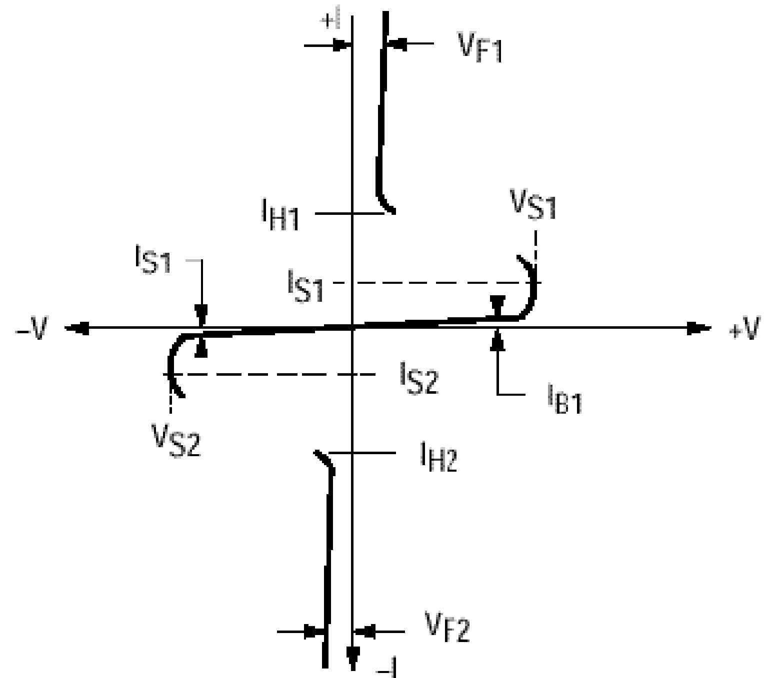
CARACTERISTICA V-I

SBS (Silicon Bidirectional Switch)

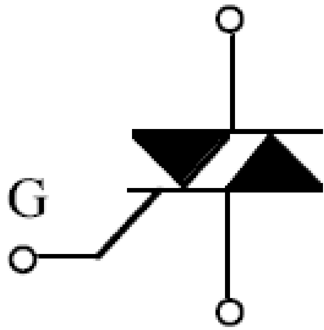


SIMBOLO

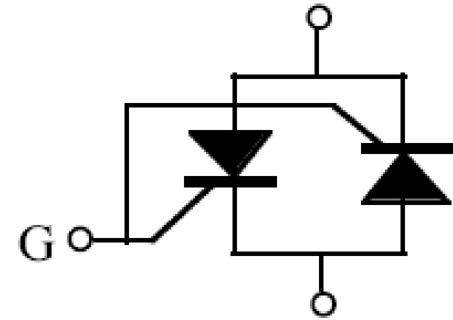




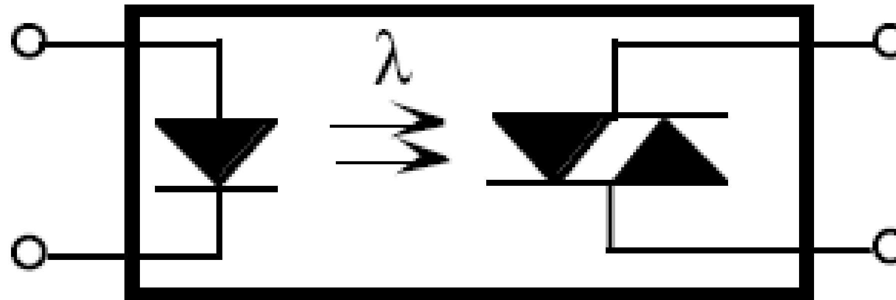
TRIAC



BIDIRECCIONAL



TRIAC CON ACOPLADOR OPTICO



APLICACIONES