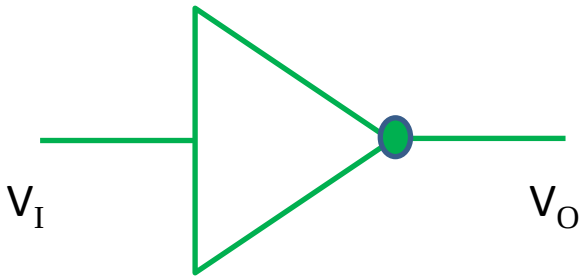
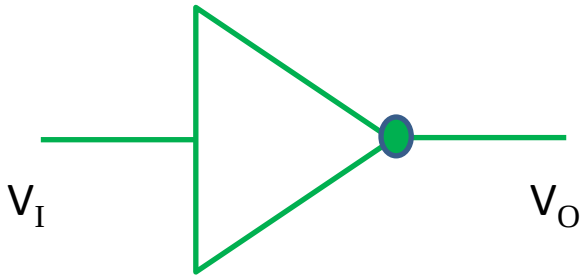
Circuitos Digitales → Niveles de tensión discretos

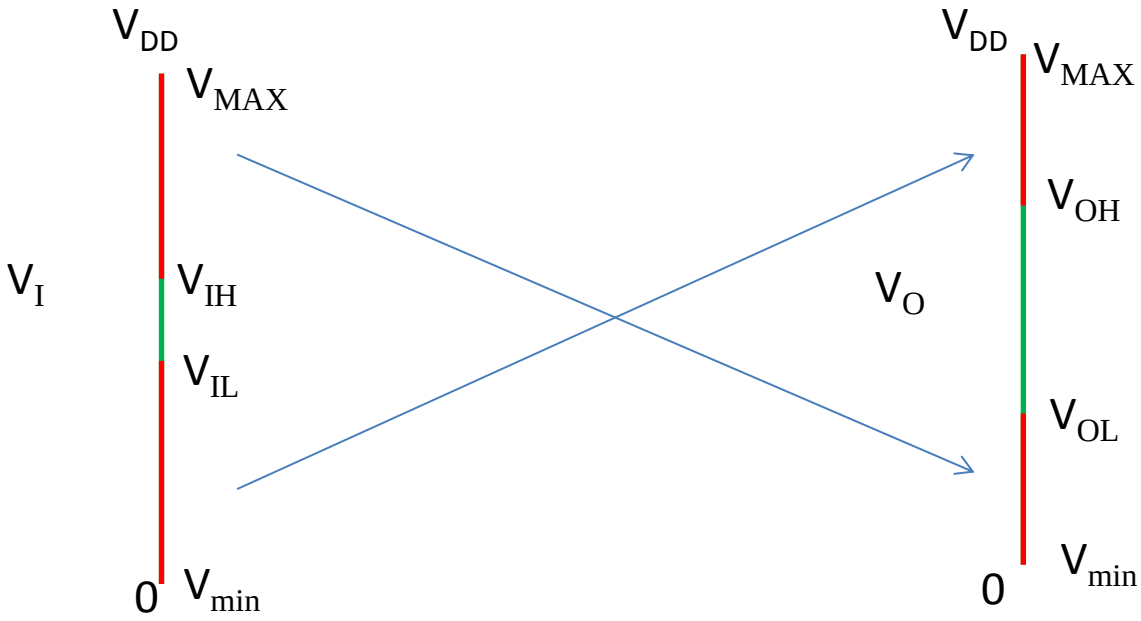
Circuitos Digitales Binarios → Dos niveles de tensión → $V_H \rightarrow 1$; $V_L \rightarrow 0$

Circuito Inversor →

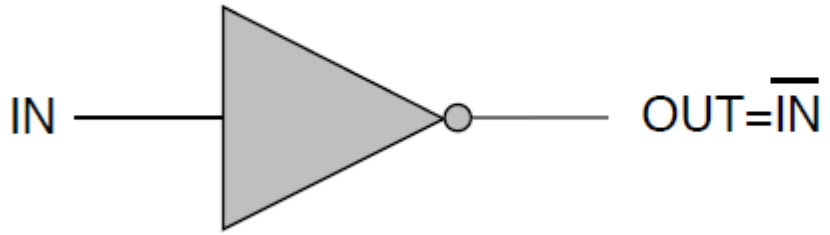


V_I	V_O
1	0
0	1

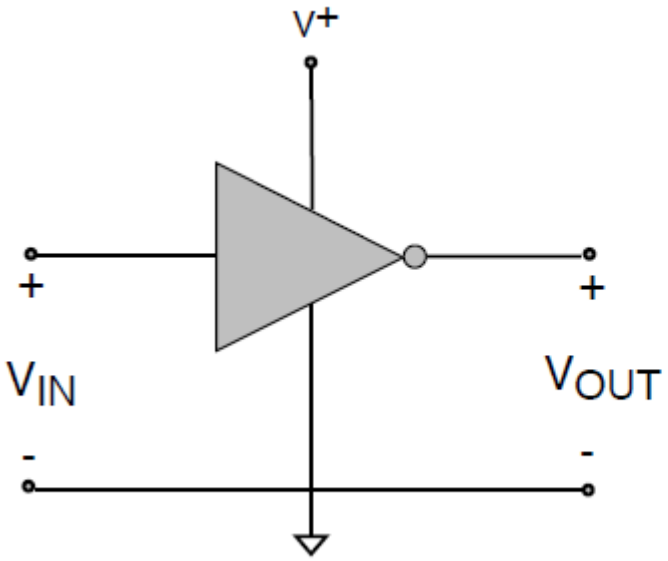

V_I
V_O

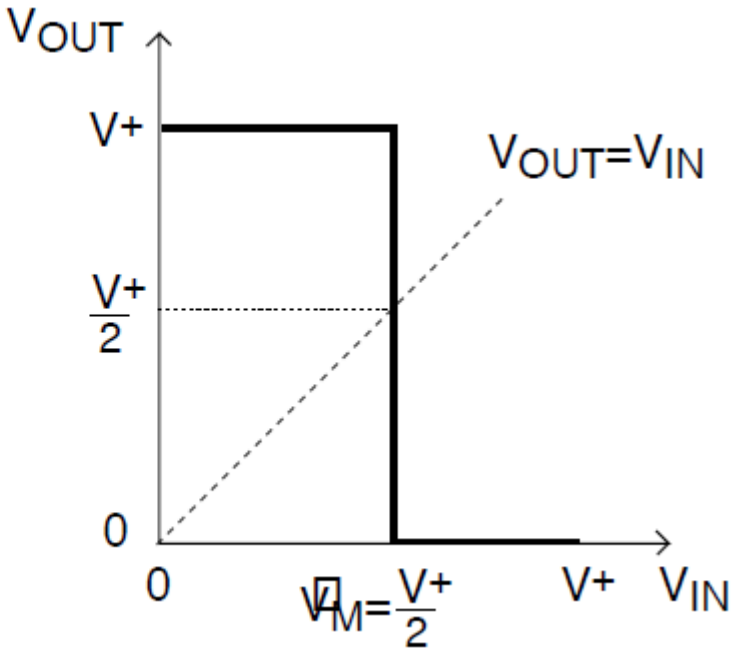

V_{DD}
V_{MAX}
V_I
V_{IH}
V_{IL}
0
V_{min}
V_{DD}
V_{MAX}
V_{OH}
V_O
V_{OL}
0
V_{min}

INVERSOR IDEAL



IN	OUT
0	1
1	0



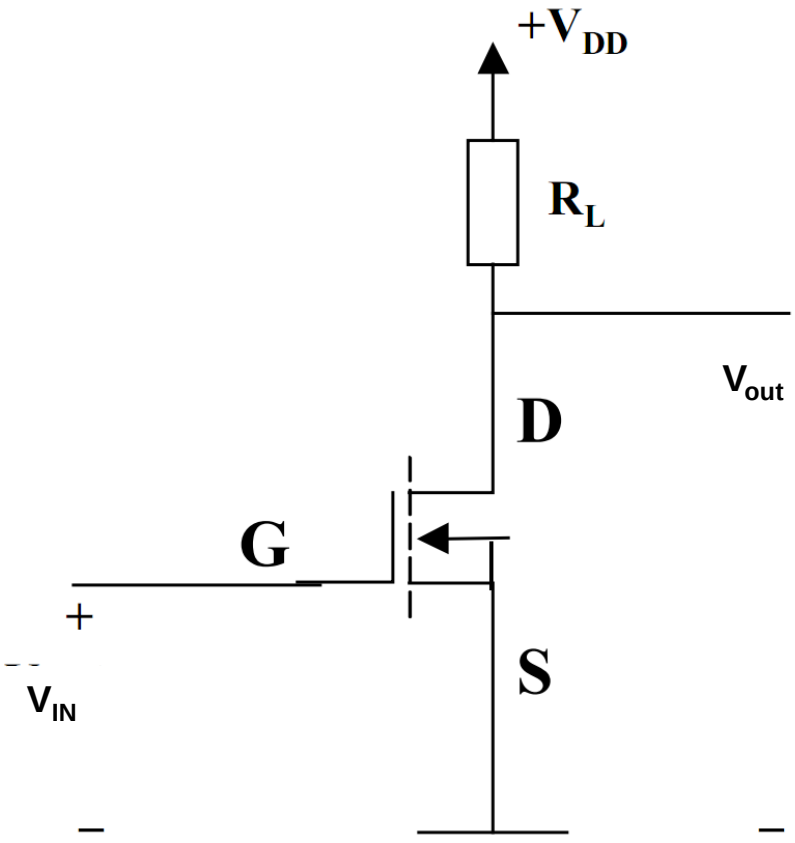


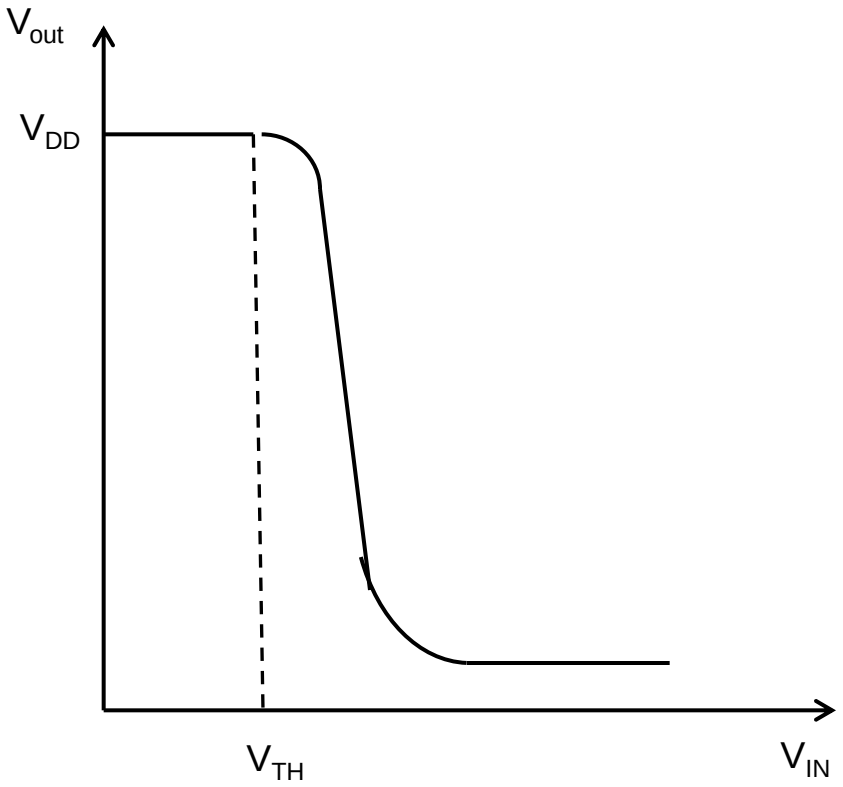
$$0 \leq V_{IN} < V_M \rightarrow V_O = V^+$$

$$V_M \leq V_{IN} < V^+ \rightarrow V_O = 0$$

V_M → Umbral lógico o Punto de transición

INVERSOR NMOS





$0 < V_{IN} < V_{TH}$ MOS → CORTADO $V_0 = V_{DD}$

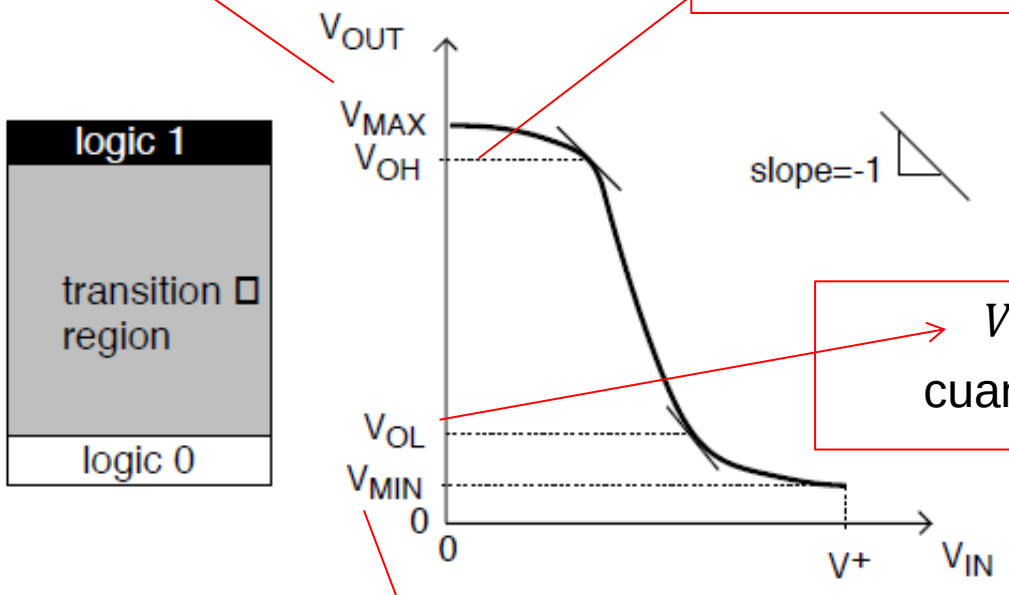
$V_{TH} < V_{IN}$ MOS → CONDUCE $V_0 = V_{DD} - I_{DS} \times R_L$

INVERSOR REAL

Niveles Lógicos

V_{MAX} *valor de* V_0 cuando $V_{IN} = 0$

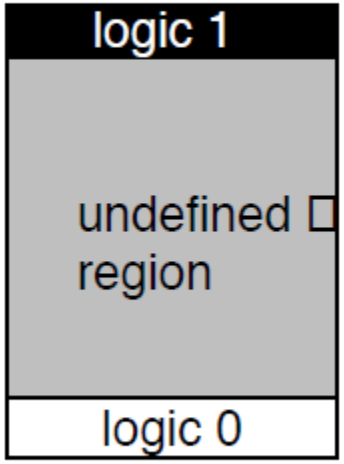
V_{OH} valor V_0 cuando $\frac{dV_0}{dV_I} = -1$

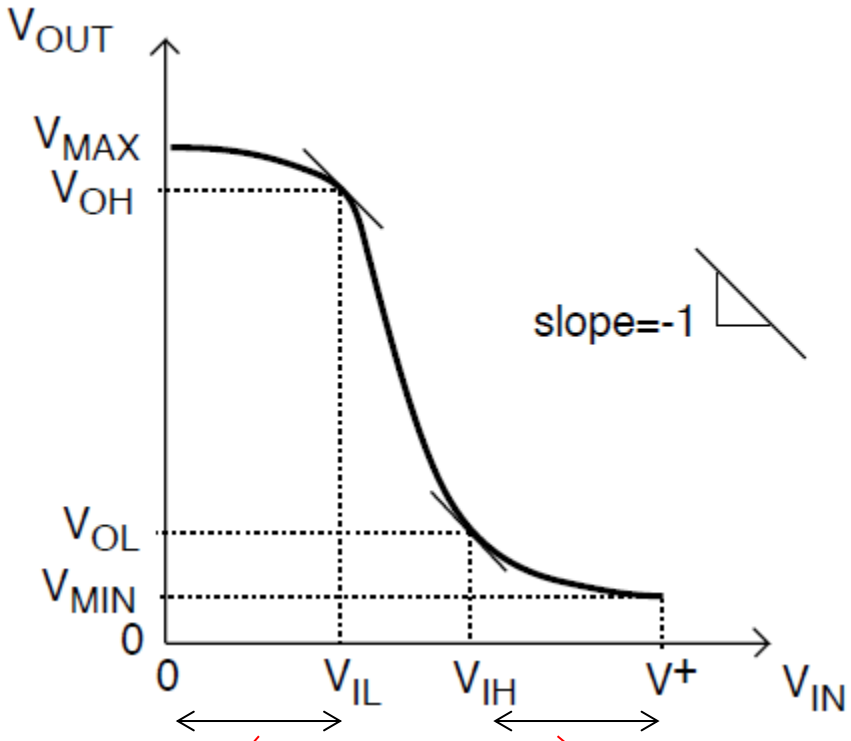


V_{OL} valor V_0 cuando $\frac{dV_0}{dV_I} = -1$

V_{MIN} *valor de* V_0 cuando $V_{IN} = V^+$

INVERSOR REAL



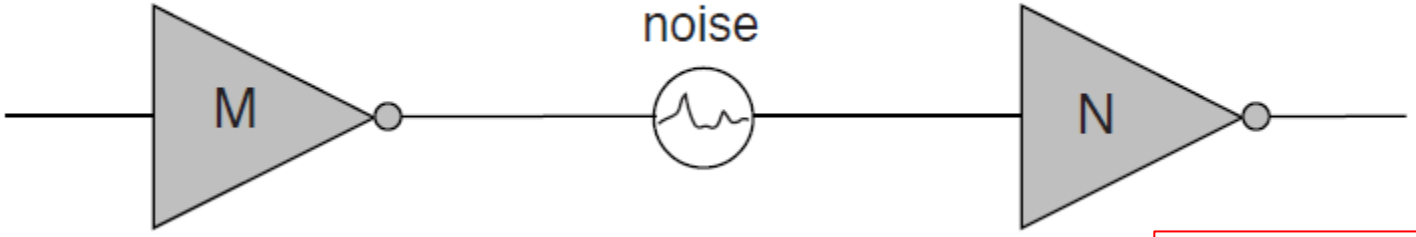


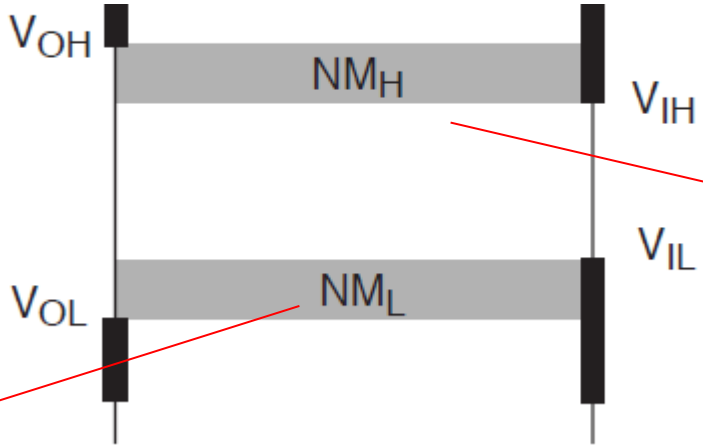
Rango de tensión V_{IN} que produce un “1” lógico de salida

Rango de tensión V_{IN} que produce un “0” lógico de salida

INVERSOR REAL

Margen de ruido





Margen de Ruido del nivel Alto

$NM_H = V_{0H} - V_{IH}$

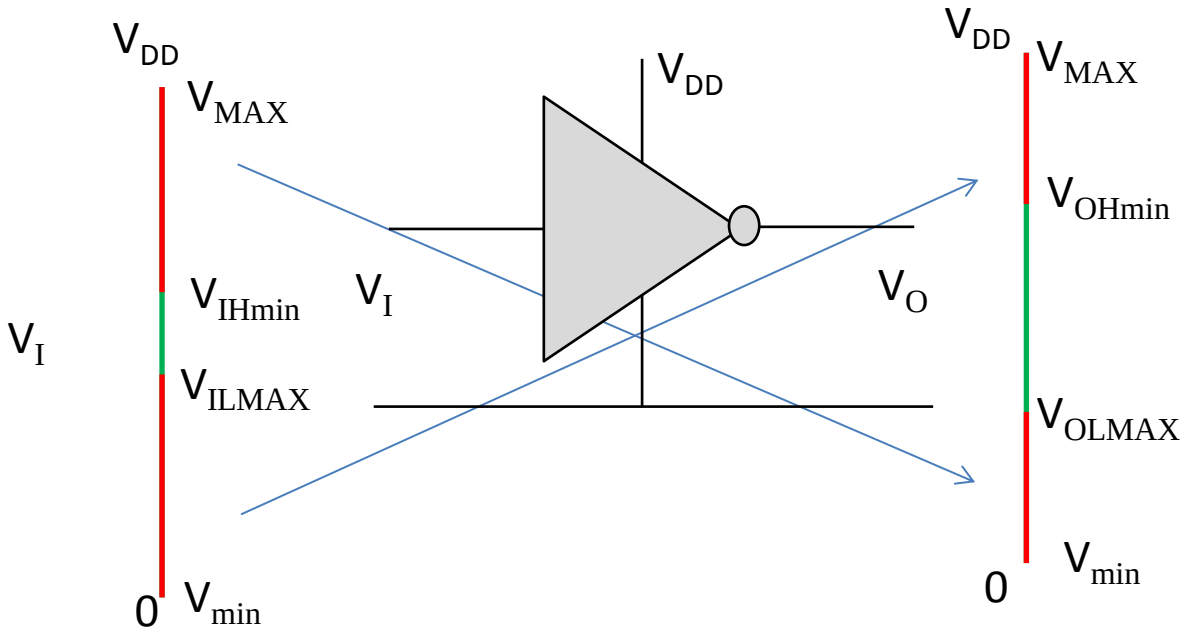
Margen de Ruido del nivel Bajo

$NM_L = V_{IL} - V_{0L}$

Inversor M
Niveles de tensión de salida

Inversor N
Niveles de tensión de entrada

El margen de ruido se calcula tomando la peor situación



Para conectar dos inversores en cascada

Nivel bajo peor caso

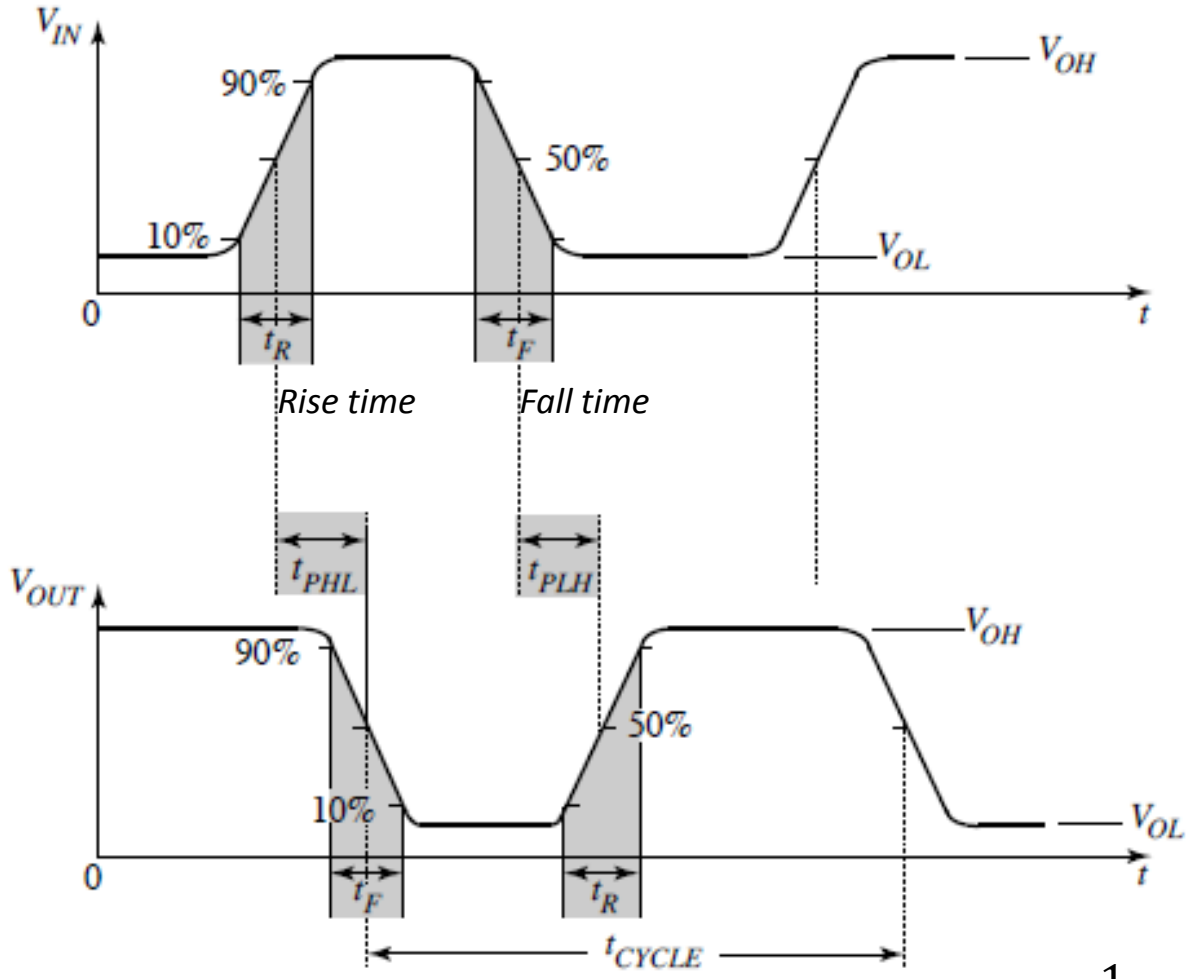
$$V_{0LMAX} \leftrightarrow V_{ILMAX}$$

Nivel alto peor caso

$$V_{0Hmin} \leftrightarrow V_{IHmin}$$

INVERSOR REAL

Tiempos de conmutación



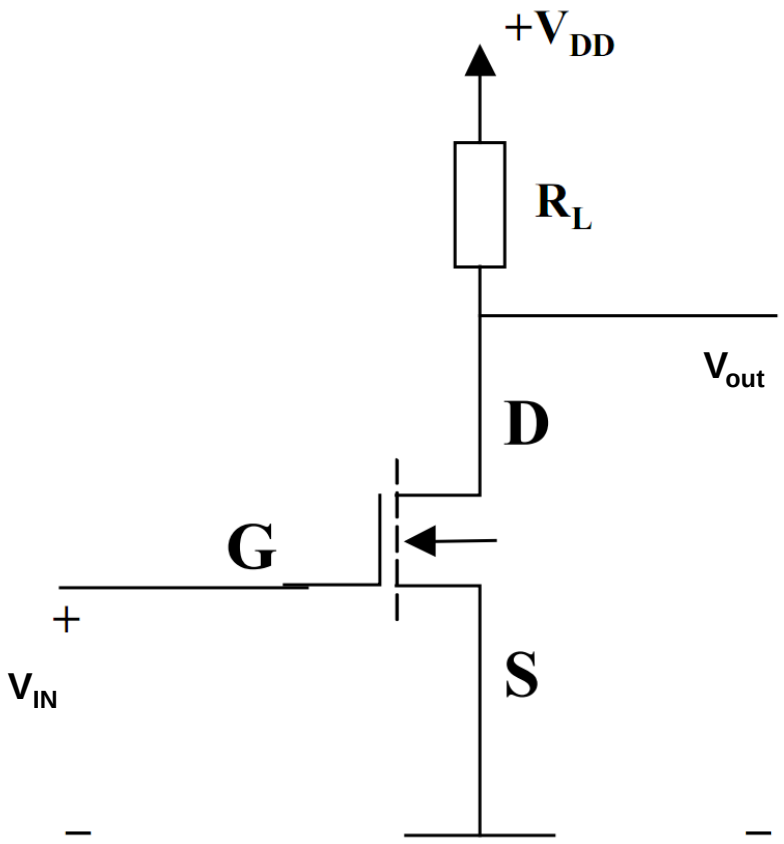
$t_{PHL} \rightarrow tiempo\ de\ conmutacion\ de\ alto\ a\ bajo$

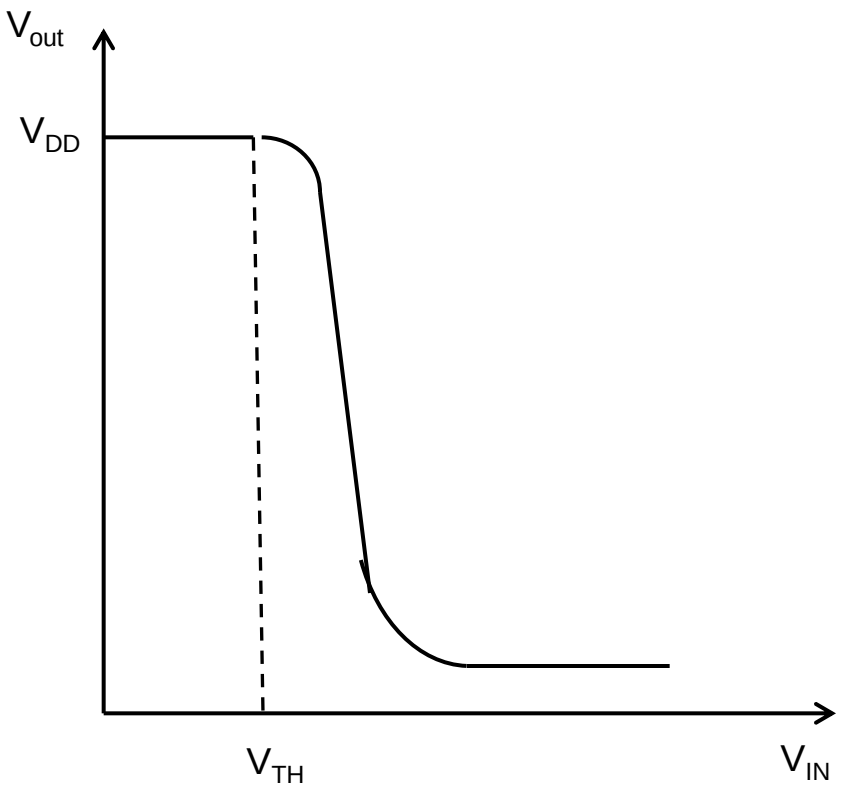
$t_{PLH} \rightarrow tiempo\ de\ conmutacion\ de\ bajo\ a\ alto$

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Retardo
de propagación

INVERSOR NMOS



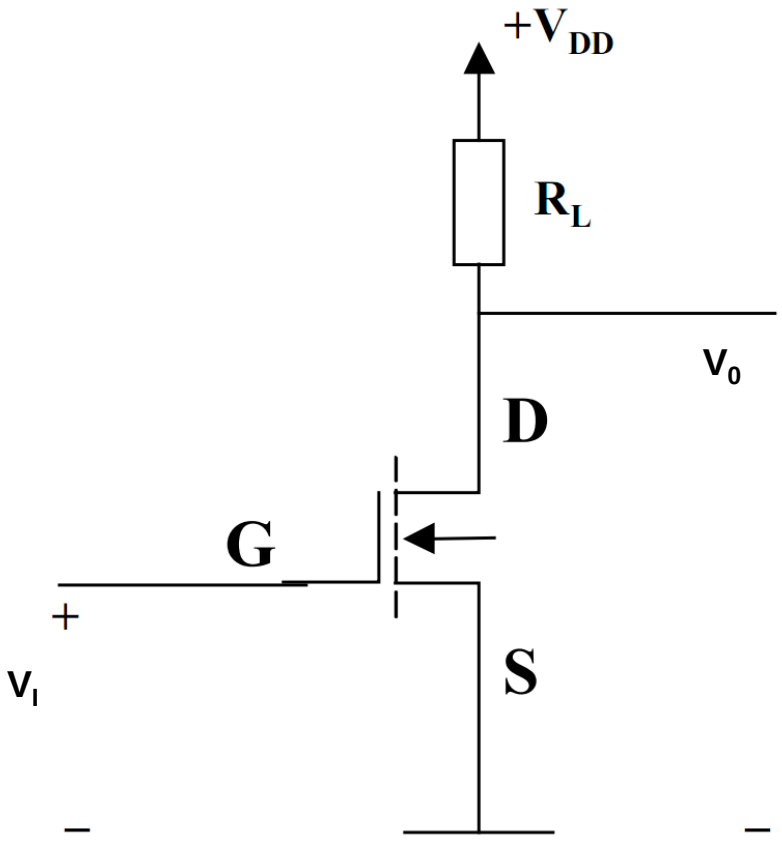


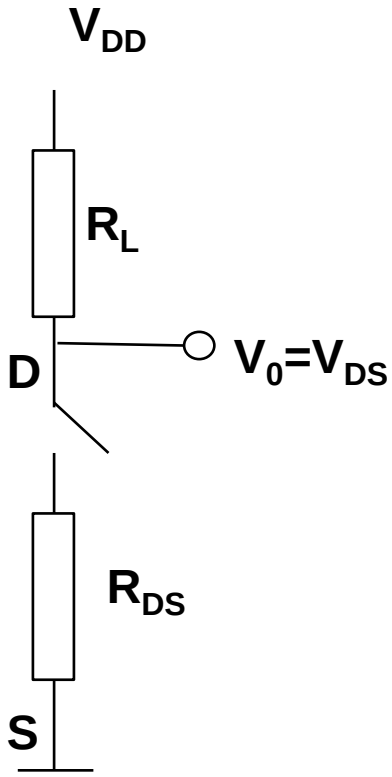
$0 < V_{IN} < V_{TH}$ MOS → CORTADO $V_0 = V_{DD} \rightarrow V_H$

$V_{TH} < V_{IN}$ MOS → CONDUCE $V_0 = V_{DD} - I_{DS} \times R_L$

I_{DS} Óhmico o Saturado Resolver desigualdad

INVERSOR NMOS



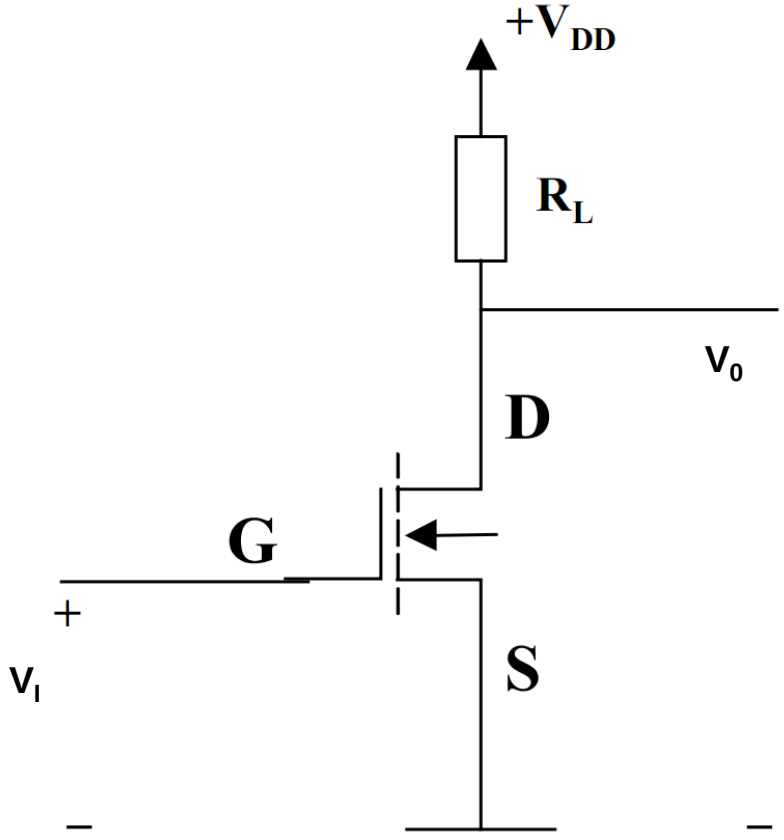


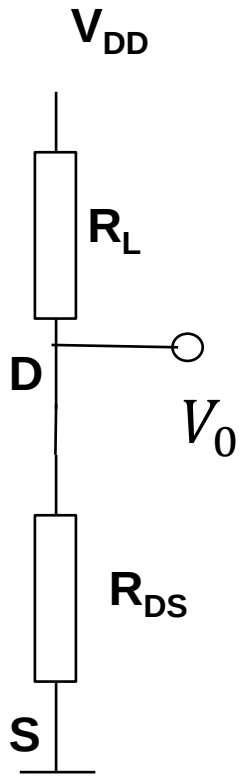
Para $V_I \leq V_{TH}$

MOS no conduce →llave abierta

$$V_0 = V_{DD} \rightarrow V_{HMAX} = V_{DD}$$

INVERSOR NMOS





Para $V_{TH} \leq V_I$

MOS conduce →llave cerrada

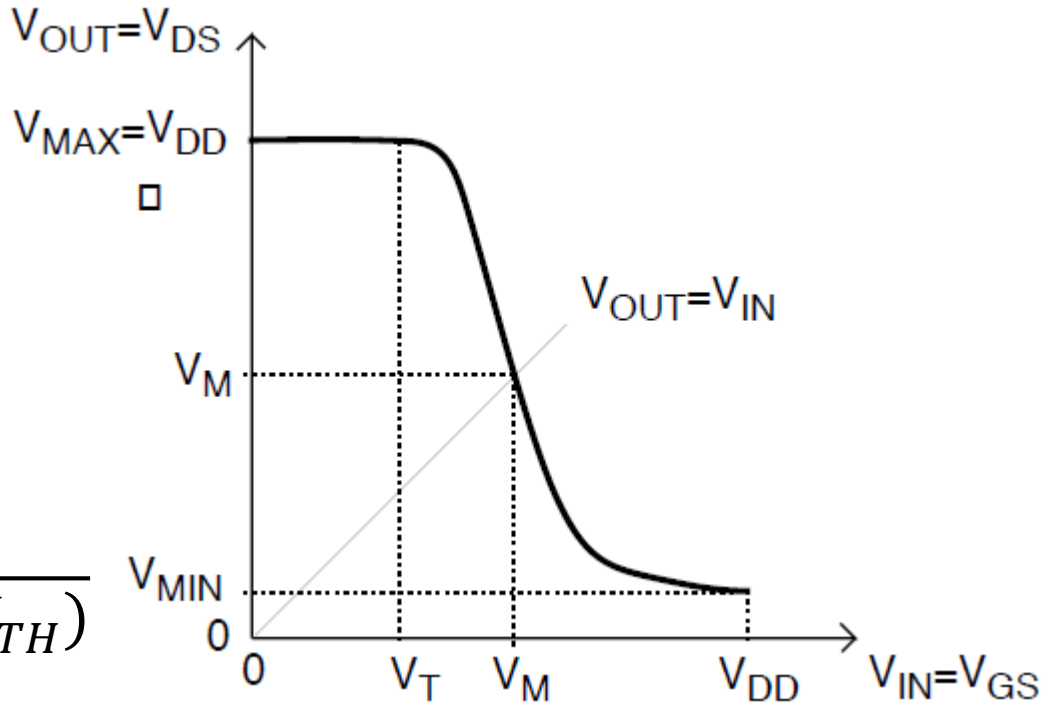
Para $V_I = V_{DD}$ si el MOS esta en zona óhmica

$$V_0 = V_{DD} \frac{R_{DS}}{R_{DS} + R_L}$$

$$R_{DS} = \frac{1}{\beta(V_{DD} - V_{TH})}$$

INVERSOR NMOS

$V_{MAX} = V_{DD}$

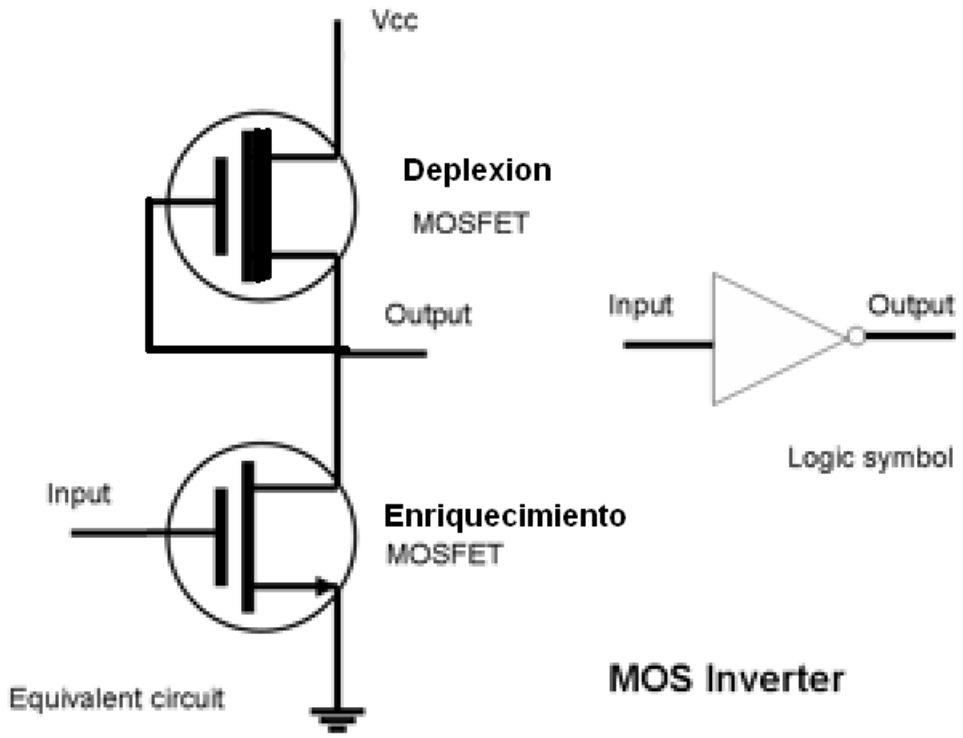


$$V_{MIN} = \frac{V_{DD}}{1 + R_L \beta (V_{DD} - V_{TH})}$$

- Para que el nivel de salida bajo sea próximo a cero

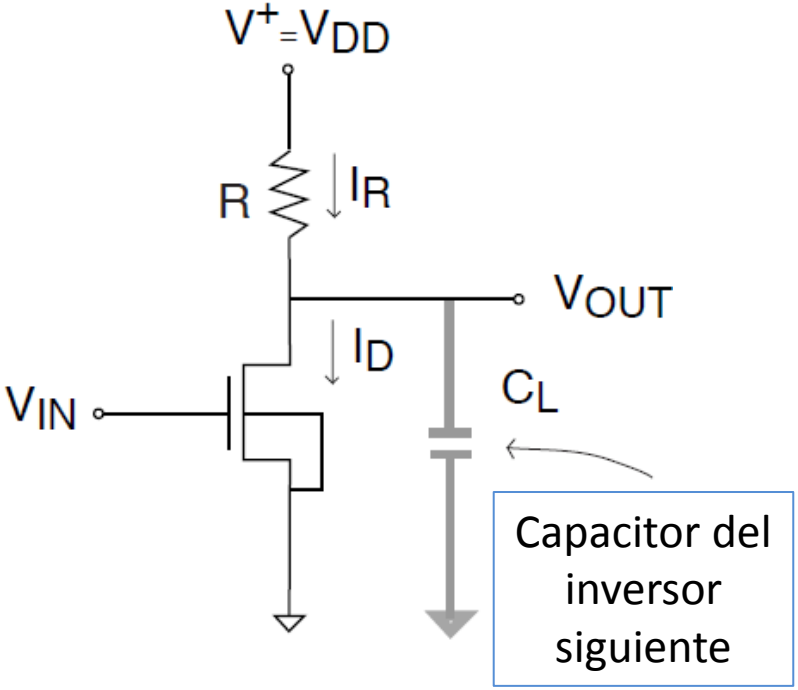
$$V_{MIN} = V_{DD} \frac{R_{DS}}{R_{DS} + R_L} \qquad R_L \gg R_{DS} \qquad V_{MIN} \approx V_{DD} \frac{R_{DS}}{R_L}$$

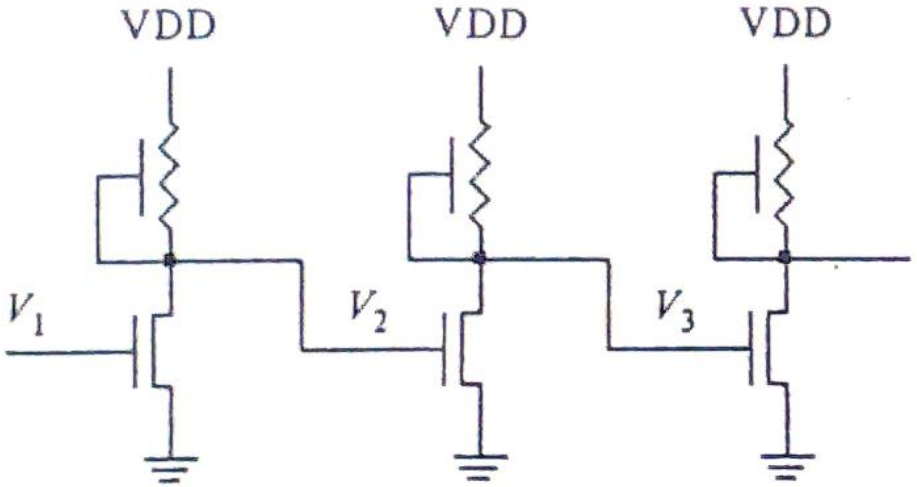
INVERSOR NMOS

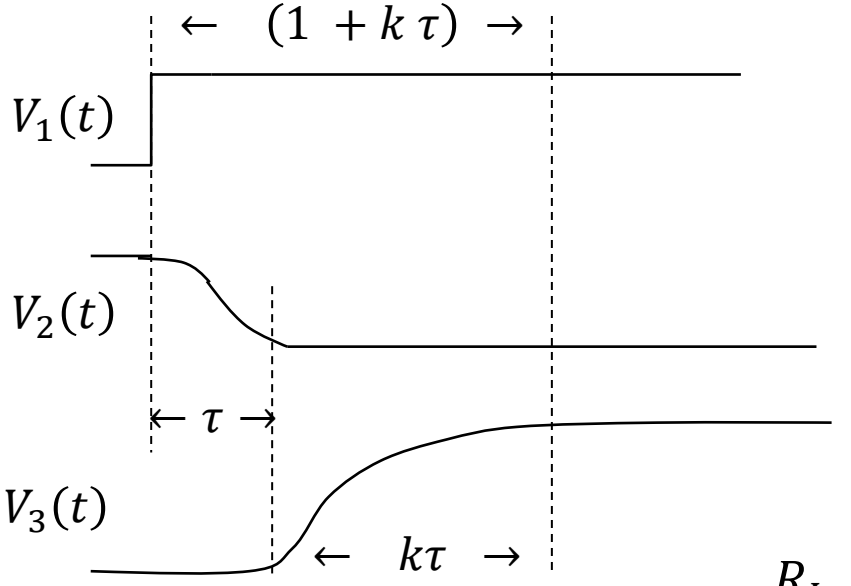


Circuito para obtener R_L de gran valor con poca área de silicio

Retardo del Inversor





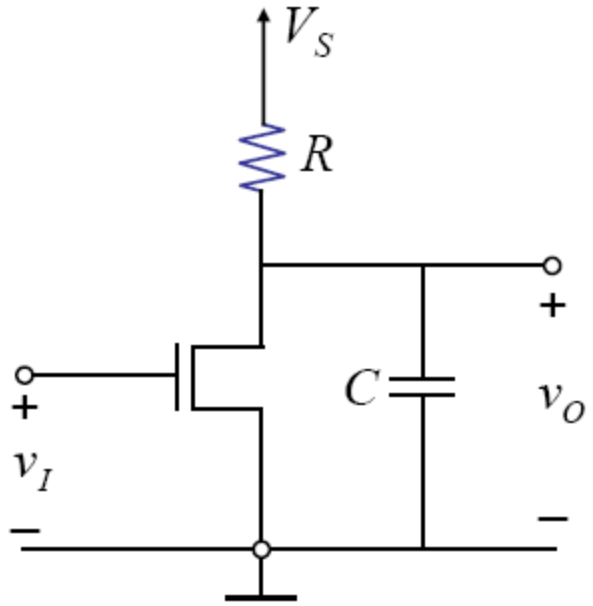


$\tau = R_{DS} \times C_L$

$k = \frac{R_L}{R_{DS}}$

Energía y potencia

Estudie la disipación de energía en las puertas del MOSFET

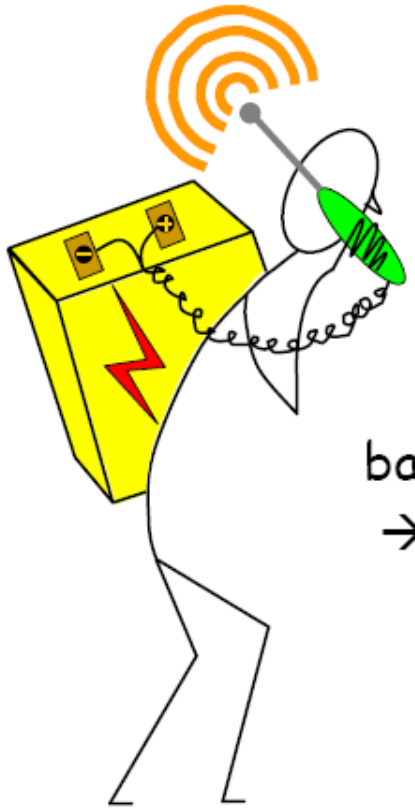


C: capacidad de cableado y
C_{GS} de la puerta siguiente

Determinemos:

- la potencia de reserva
- la potencia activa

¿Por qué preocuparnos por la energía?

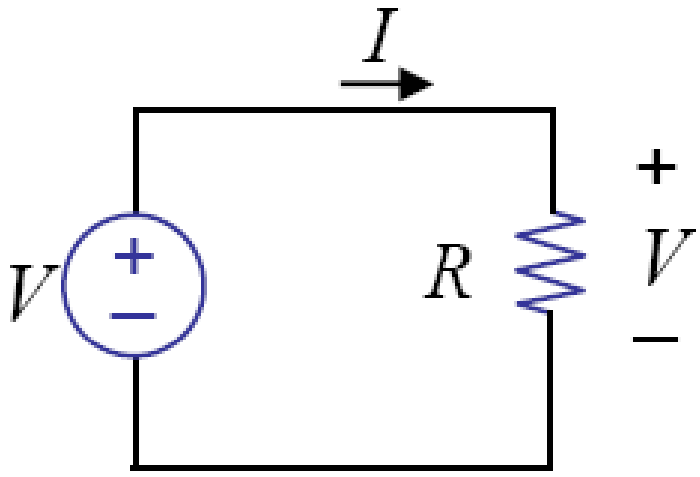


baterías pequeñas
→ bueno

Hoy:

- ¿Cuánto durará la batería?
  - en modo de reserva
  - en uso activo
- ¿Se recalentará el chip y se autodestruirá?

Ejemplo 1:

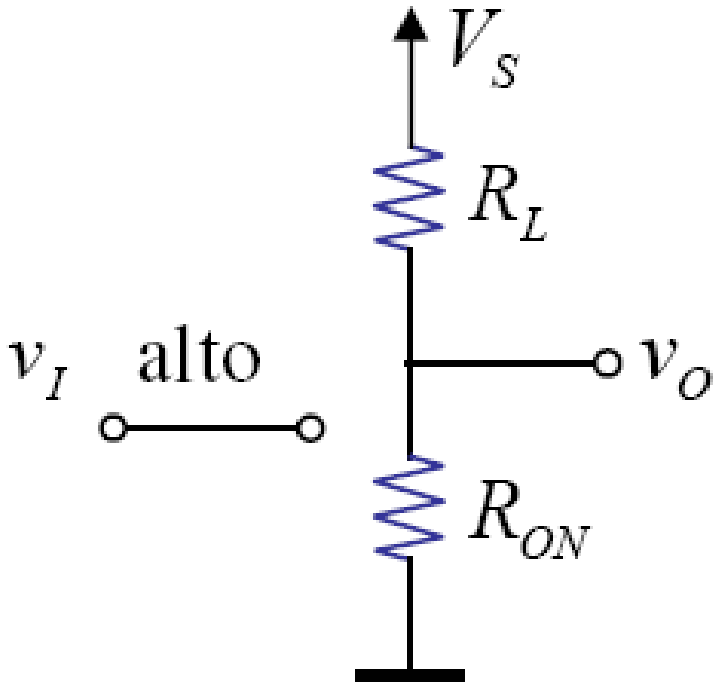


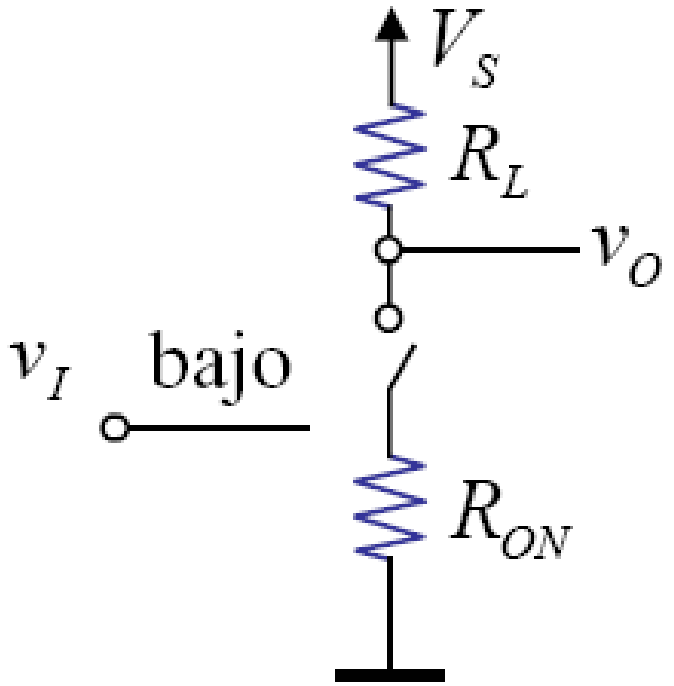
Potencia, $P = VI = \frac{V^2}{R}$

Energía disipada en tiempo T

$$E = VIT$$

Para nuestra puerta:



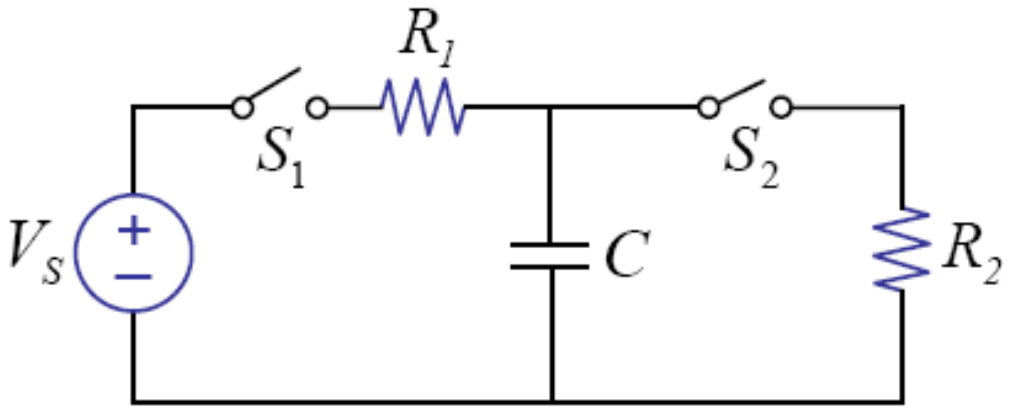


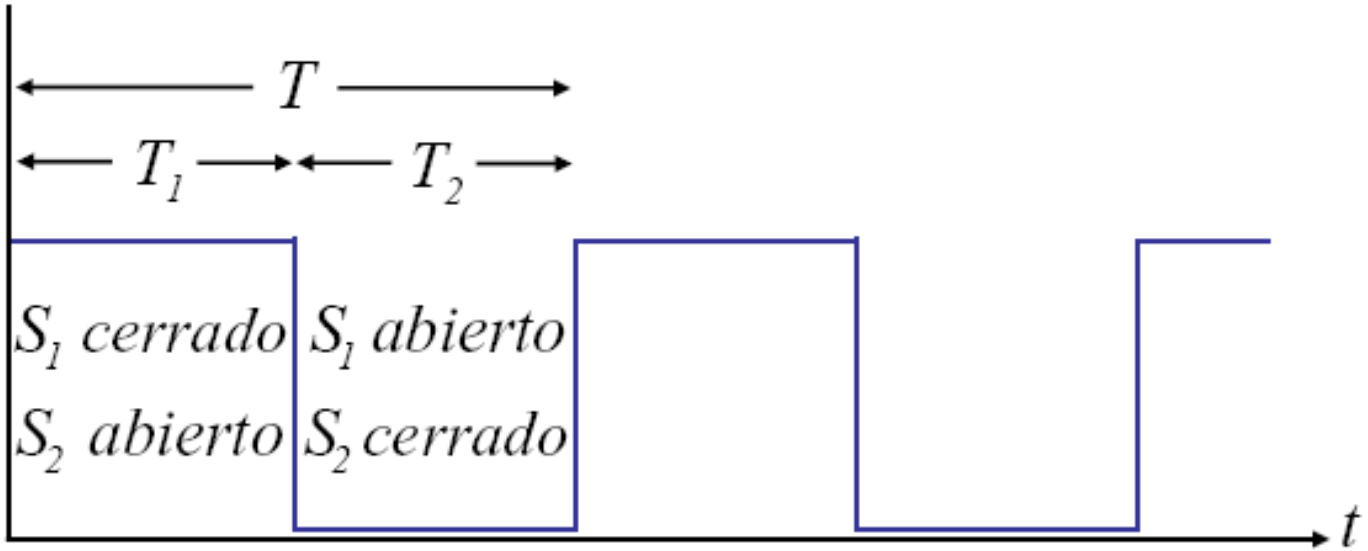
$$P = \frac{V_S^{\,2}}{R_L + R_{ON}}$$

$$P = 0$$

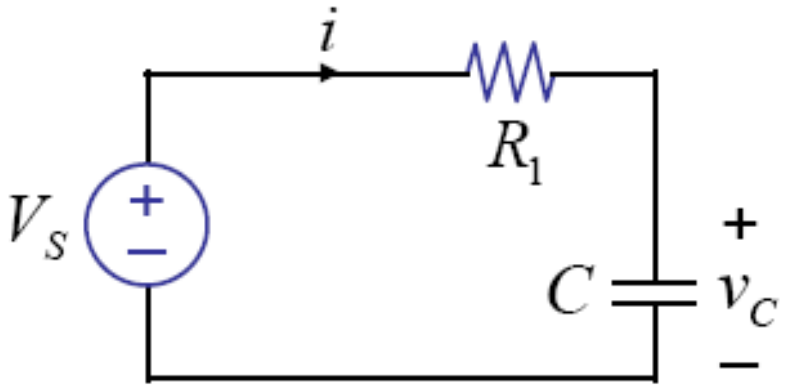
Ejemplo 2:

Considere:

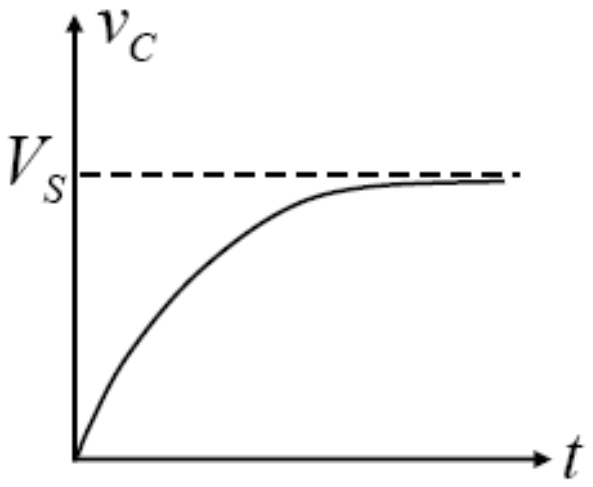


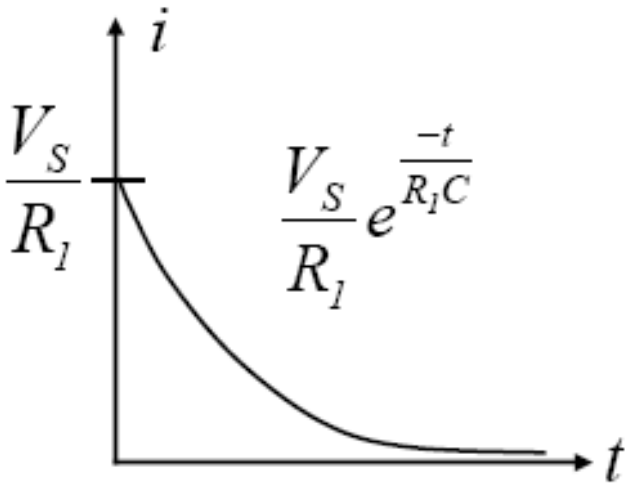


T_1: S_1 cerrado, S_2 abierto



suponga que,
$v_C = 0$ en $t = 0$





Energía total que proporciona una fuente durante T_1

$$E = \int_0^{T_1} V_S i \, dt$$

$$= \int_0^{T_1} \frac{V_S^{\,2}}{R_1} e^{\frac{-t}{R_1 C}} dt$$

$$= -\frac{V_S^{\,2}}{R_1} R_1 C \, e^{\frac{-t}{R_1 C}} \Big|_0^{T_1}$$

$$= C V_S^{\,2} \left(1 - e^{\frac{-T_1}{R_1 C}} \right)$$

$$\approx C V_S^{\,2} \quad si \quad T_1 >> R_1 C$$

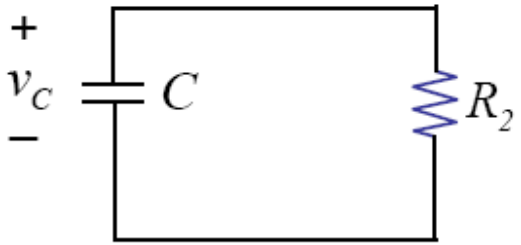
es decir, si esperamos lo suficiente

$\frac{1}{2} C V_S^{\,2}$ *almacenado en C,*

$E_1 = \frac{1}{2} C V_S^{\,2}$ *disipado en* R_1

} Independiente de R

T_2: S_2 cerrado, S_1 abierto



En un principio, $v_C = V_S$ (recuerde $T_1 >> R_1C$)

Por lo tanto, inicialmente,

energía almacenada en condensador $= \frac{1}{2} C V_S^{\,2}$

Suponga que $T_2 >> R_2C$

Por tanto, el condensador se descarga ~completamente en T_2

Por tanto, la energía disipada en R_2 durante T_2,

$$E_2 = \frac{1}{2} C V_S^{\,2}$$

E_1, E_2 independiente de R_2

Juntando los dos:

Energía disipada en cada ciclo,

$$E = E_1 + E_2$$

$$= \frac{1}{2} C V_s^{\,2} + \frac{1}{2} C V_s^{\,2}$$

$$E = C V_s^{\,2} \quad \textit{energía disipada en la carga y descarga de } C$$

Supone que C se carga y se descarga completamente.

Potencia media,

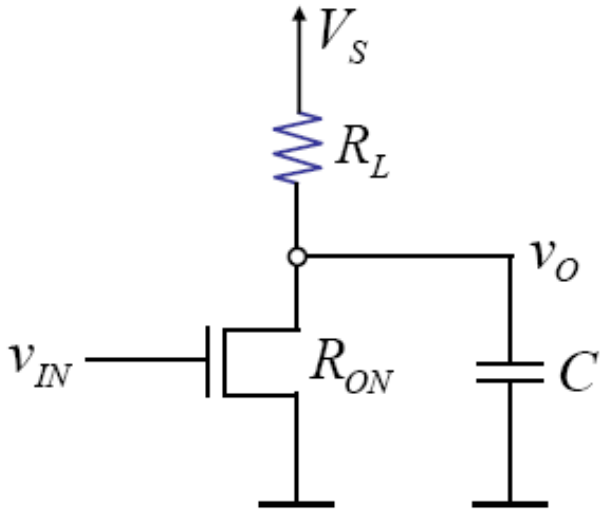
$$\overline{P} = \frac{E}{T}$$

$$= \frac{CV_s^{\,2}}{T}$$

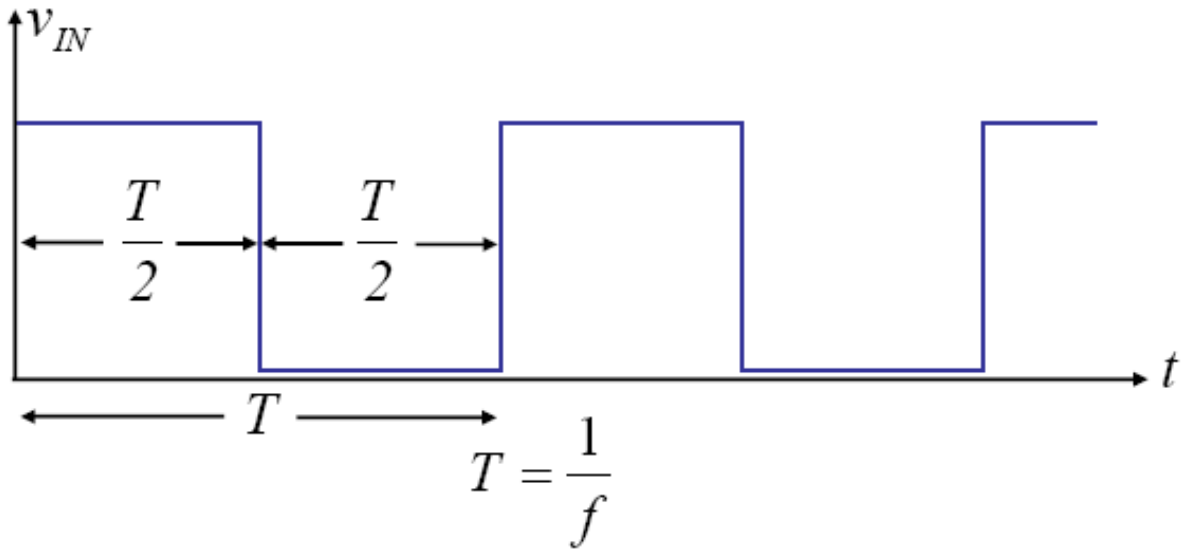
$$= CV_s^{\,2} f$$

frecuencia $f = \frac{1}{T}$

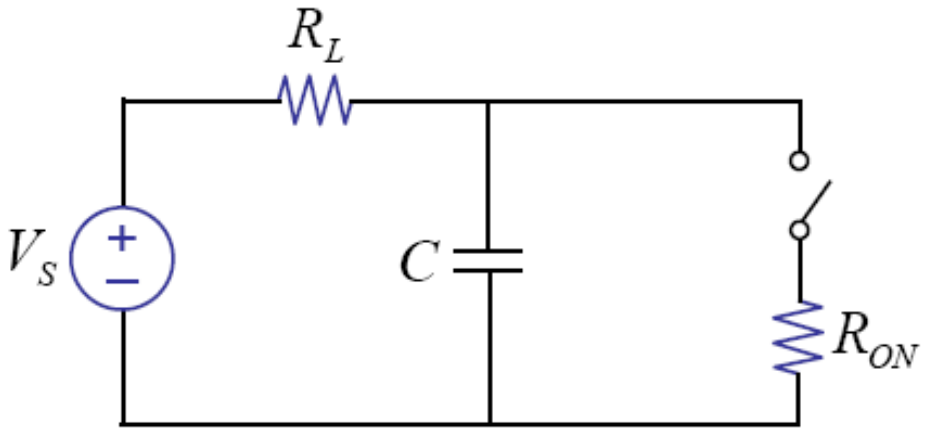
Volvemos a nuestro inversor —



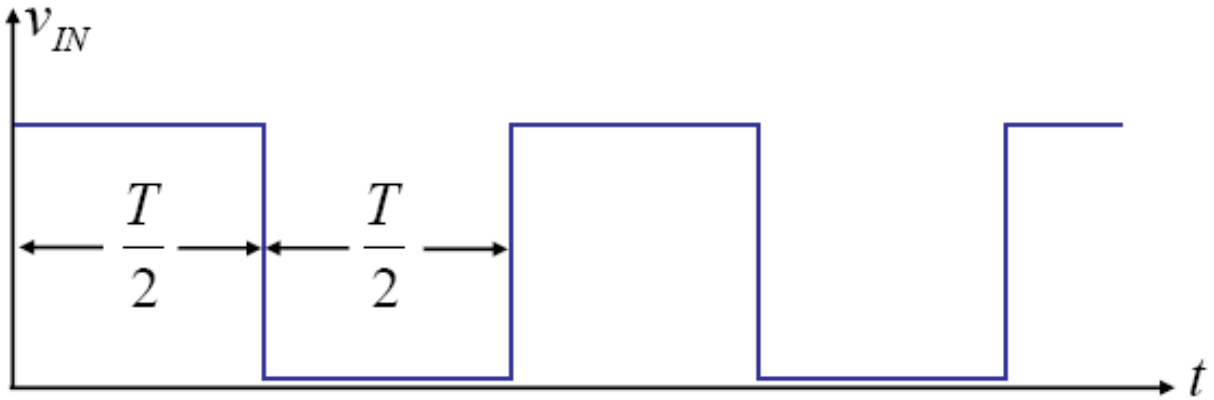
¿Qué es $\overline{P}$ para la entrada siguiente?



Circuito equivalente



¿Qué es $\overline{P}$ para la entrada siguiente?



$$T = \frac{1}{f}$$

¿Qué es $\overline{P}$ para la puerta?

Cuando $R_L >> R_{ON}$

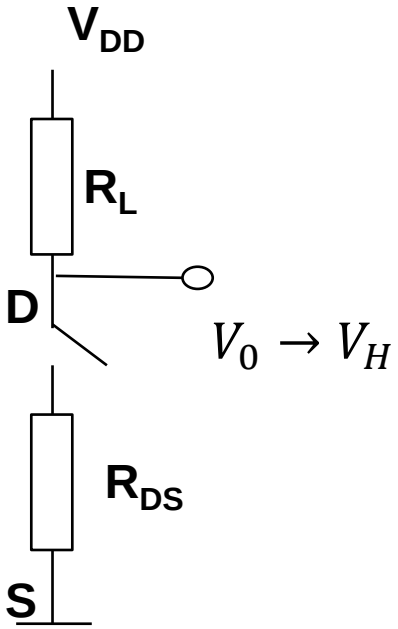
$$\overline{P} = \frac{V_S^{\,2}}{2R_L} + CV_S^{\,2} f$$

En modo de reserva, se puede suponer que la mitad de las puertas en un chip están ON. Por tanto, $\overline{P}_{ESTÁTICO}$ por puerta es $\frac{V_S^2}{2R_L}$.

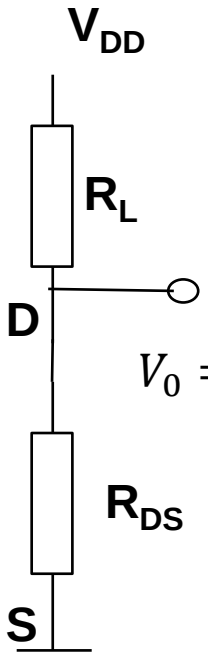
Está relacionado con la potencia de reserva.

En modo de reserva, $f \rightarrow 0$, por lo que la potencia dinámica es 0

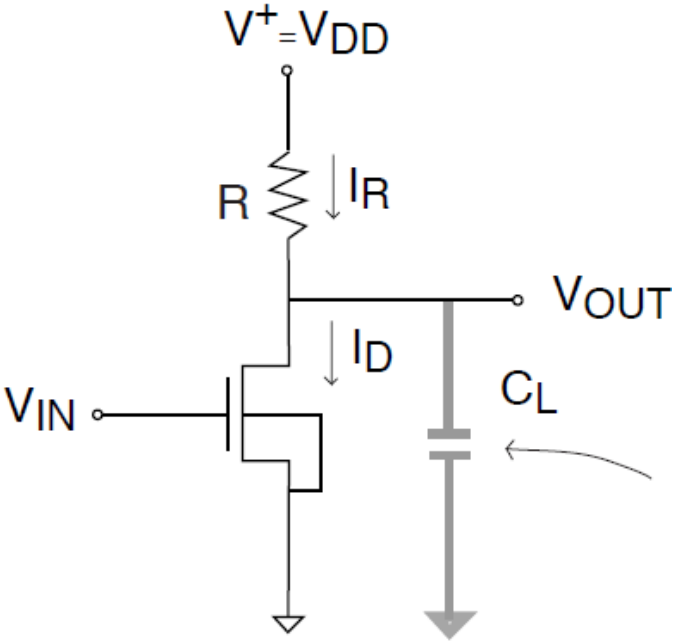
Potencia



$V_0 \rightarrow V_H$



$V_0 = V_{DD} \dfrac{R_{DS}}{R_{DS} + R_L}$



$P_{E1} = 0$

$P_{E2} = \dfrac{V_{DD}^2}{R_{DS} + R_L}$

$P_D = C_L V_{DD}^2 \times f$

$P_E = \dfrac{P_{E1} + P_{E2}}{2}$

$P_E = \dfrac{1}{2} \dfrac{V_{DD}^2}{(R_{DS} + R_L)}$

$P \approx \dfrac{V_{DD}^2}{2R_L} + C_L V_{DD}^2 \times f$

$P = P_E + P_D$

Algunos números...

Un chip con 10^6 puertas cronometrando a 100 MHZ

$$C = 1f\,F$$
$$R_L = 10\,k\Omega$$
$$f = 100 \times 10^6$$
$$V_S = 5V$$

$$\overline{P} = 10^6 \left[\frac{25}{2 \times 10^4} + 10^{-15} \times 25 \times 100 \times 10^6 \right]$$

$$= 10^6 \; [1.25\ milivatios \; + \; 2.5\ microvatios]$$

¡problema!

$1.25KW!$ — debe deshacerse de esto

$2.5W$ — no está mal

$\alpha\, V_S^{\,2}$

$\alpha\, f$

reduzca V_S

$5V \rightarrow 1V$

$2.5W \rightarrow 150\,mW$

INVERSOR NMOS

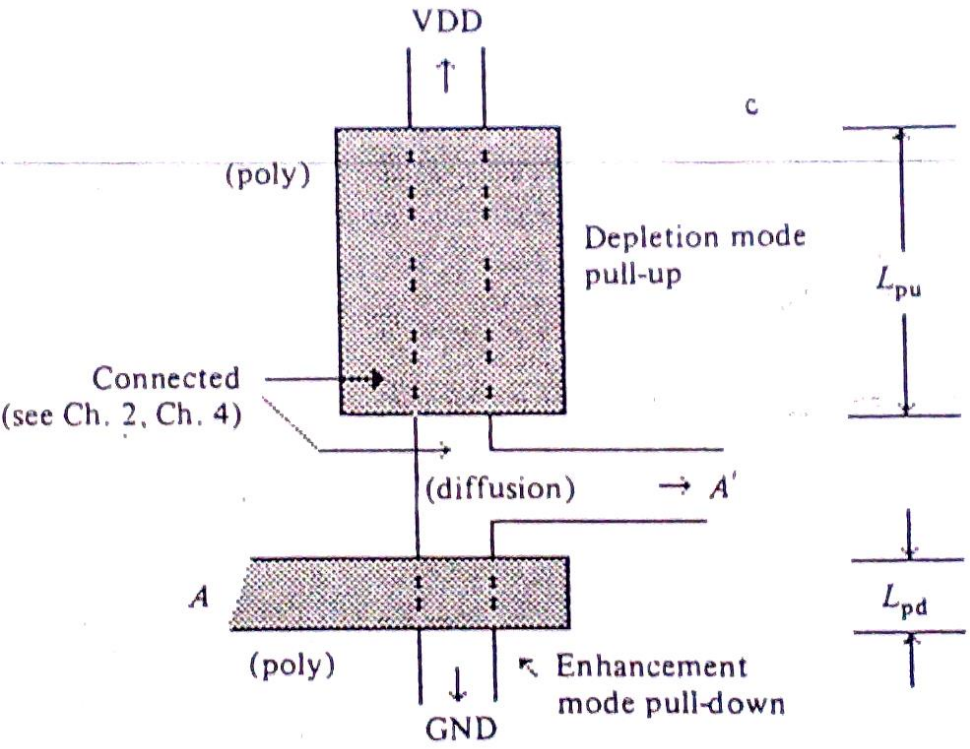
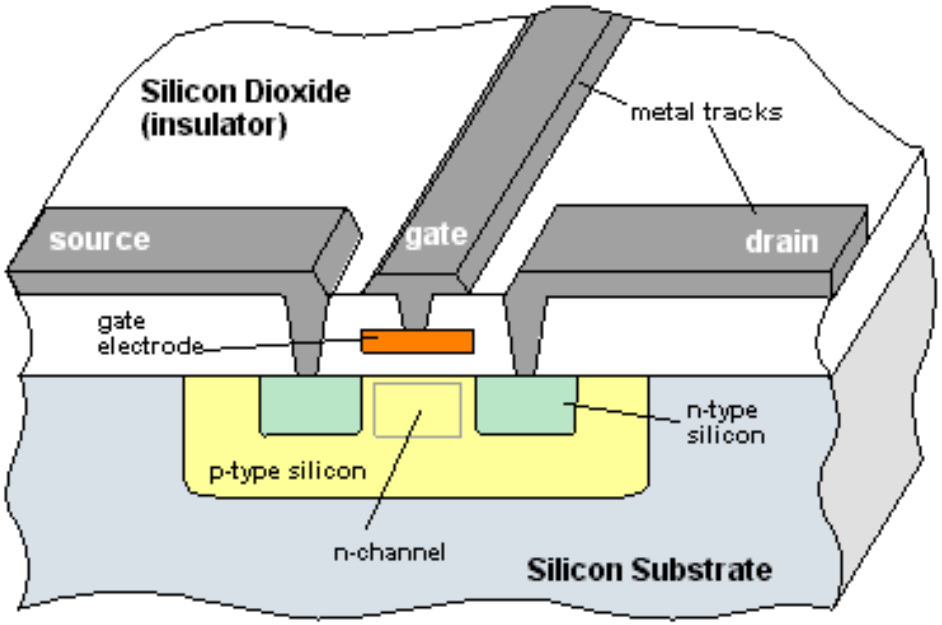


Fig. 1.8 Basic inverter layout.



Compuerta NAND

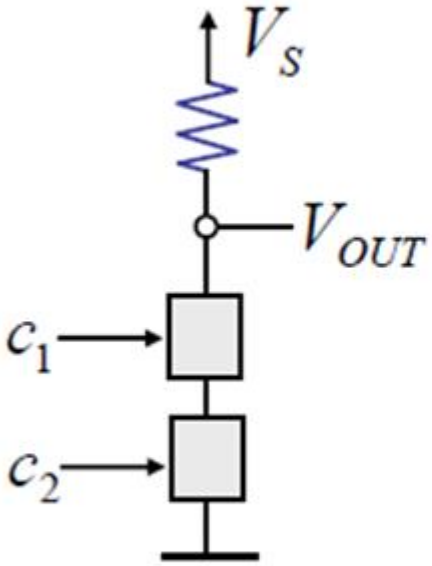
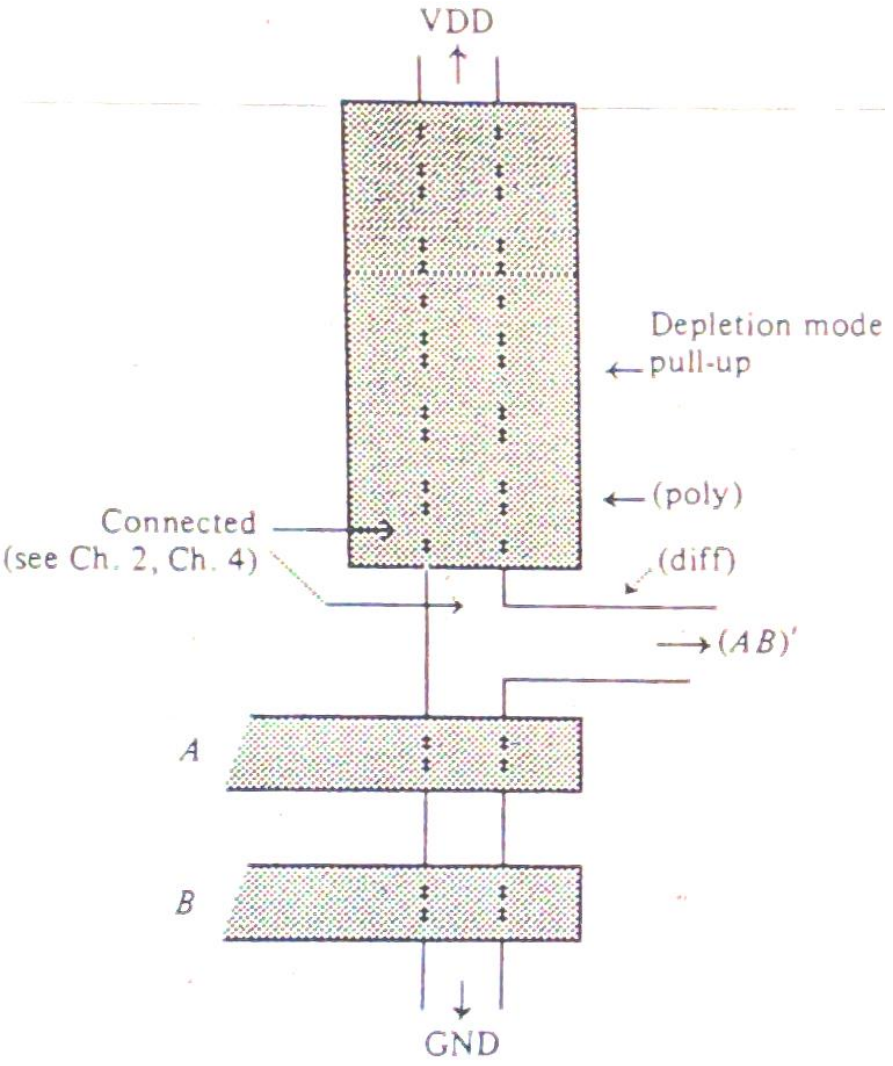
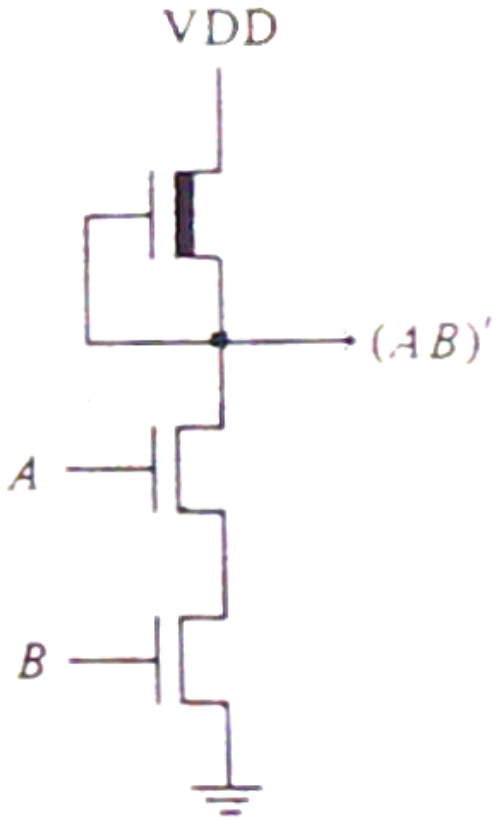


Tabla de verdad para

c_1	c_2	V_O
0	0	1
0	1	1
1	0	1
1	1	0

Compuerta NAND





A	B	(AB)'
0	0	1
0	1	1
1	0	1
1	1	0

Compuerta NOR

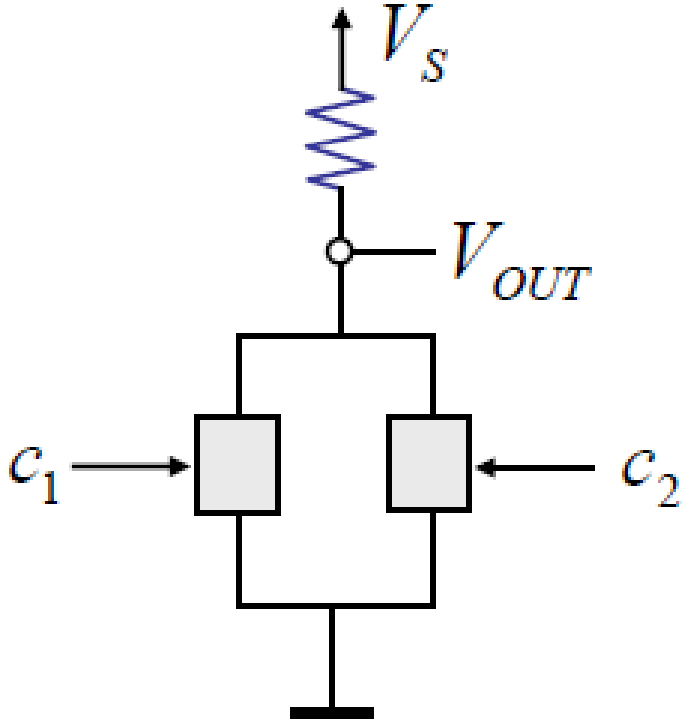
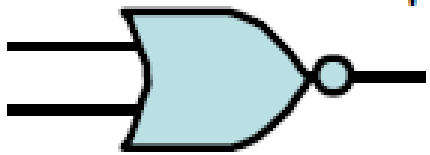
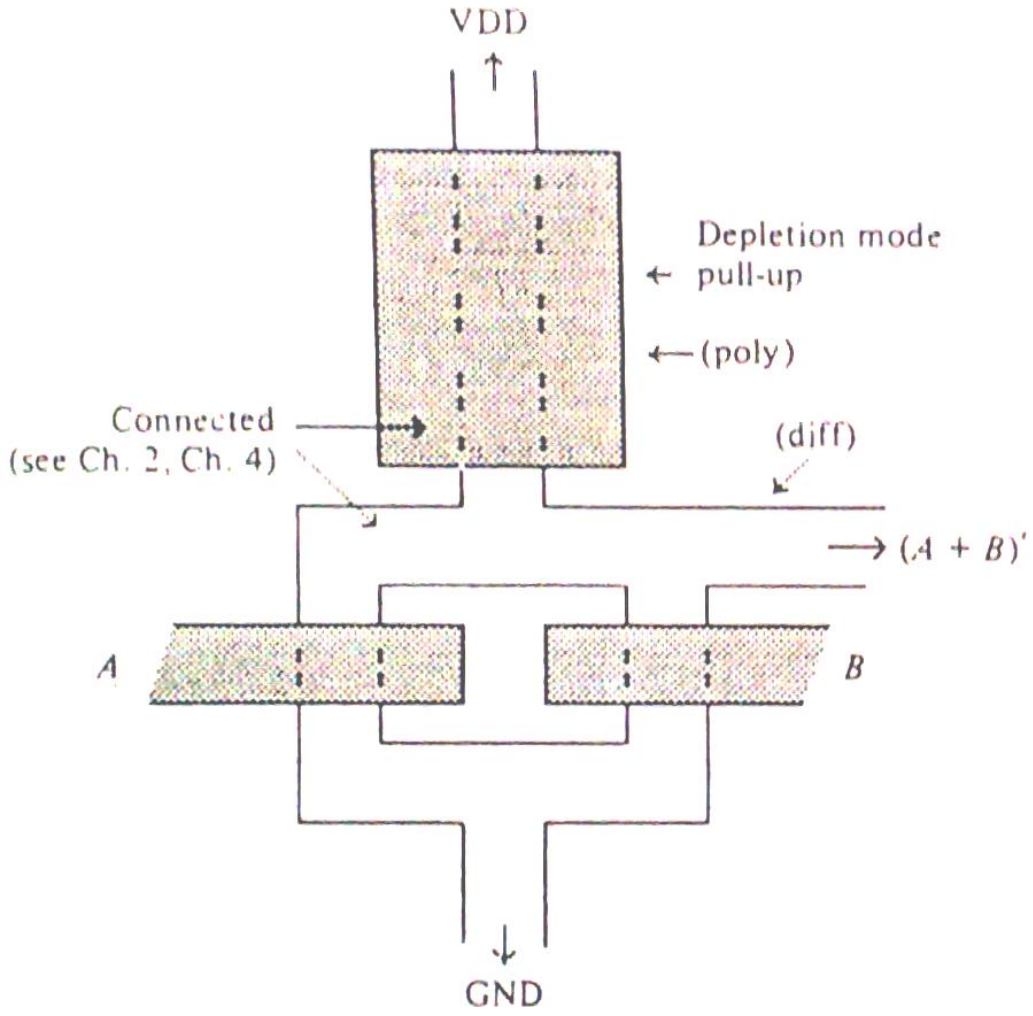


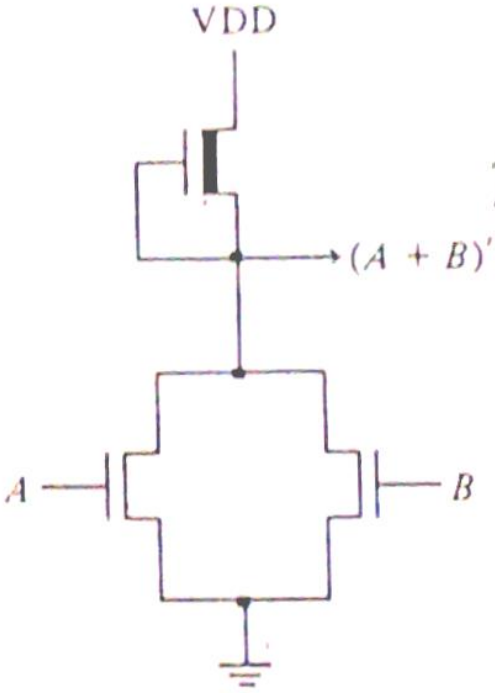
Tabla de verdad para



c_1	c_2	V_O
0	0	1
0	1	0
1	0	0
1	1	0

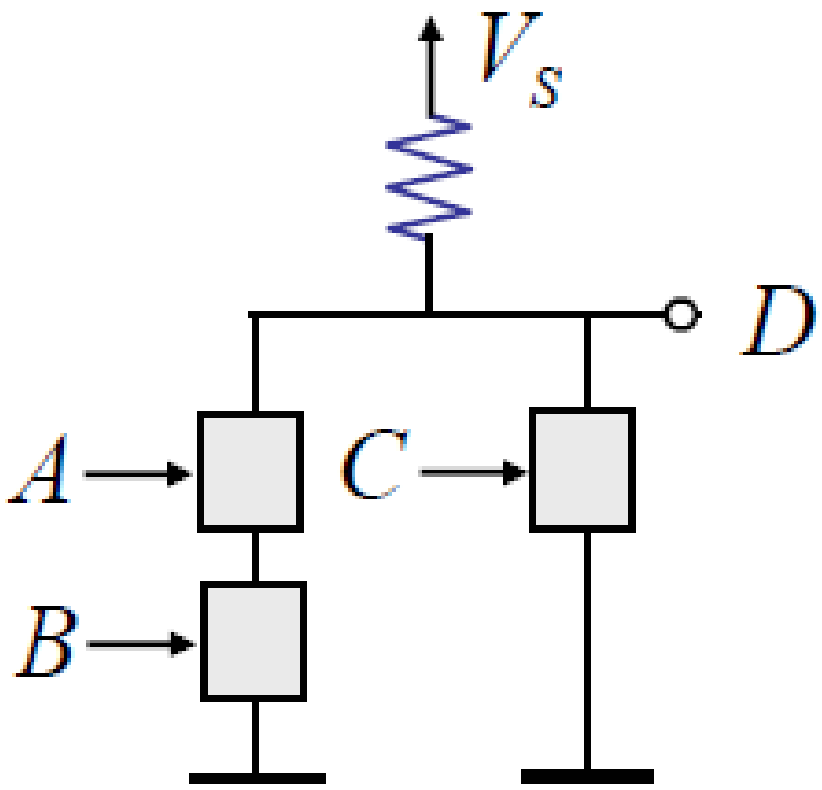
Compuerta NOR





A	B	(A + B)'
0	0	1
0	1	0
1	0	0
1	1	0

Función LOGICA



$$D = \overline{(A \cdot B) + C}$$

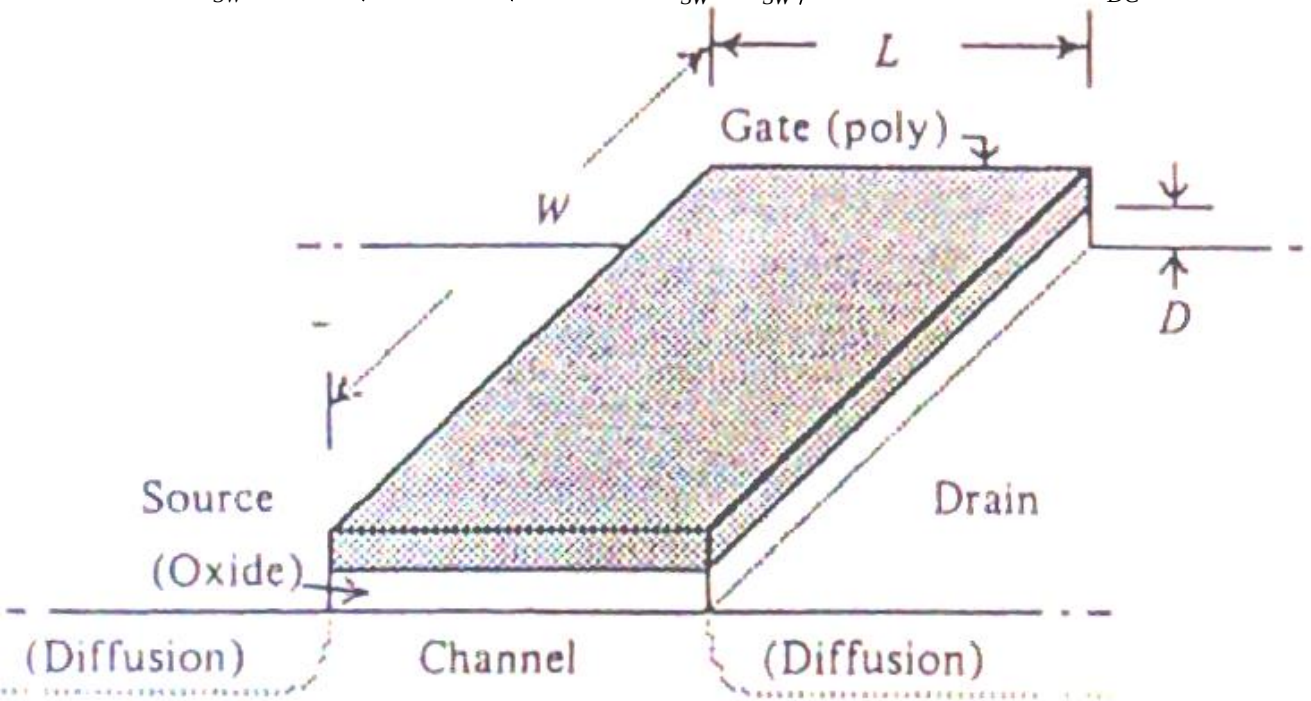
Efectos debido a la miniaturización de los circuitos MOS

$\tau \propto L^2/V$ $\quad \tau'/\tau = \left[(L/\alpha)^2/(V/\alpha)\right]/(L^2/V)$ $\quad \tau' = \tau/\alpha$

$C \propto LW/D$ $\quad C'/C = \left[(L/\alpha)(W/\alpha)/(D/\alpha)\right]/(LW/D)$ $\quad C' = C/\alpha$

$I \propto WV^2/LD$ $\quad I'/I = \left[(WV^2/\alpha^3)/(LD/\alpha^2)\right]/(WV^2/LD)$ $\quad I' = I/\alpha$

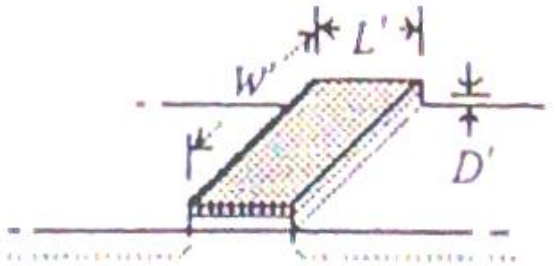
$P_{SW} \propto CV^2/\tau \propto WV^3/DL$ $\quad P'_{SW} = P_{SW}/\alpha^2$ $\quad P_{DC} = IV$ $\quad P'_{DC} = P_{DC}/\alpha^2$



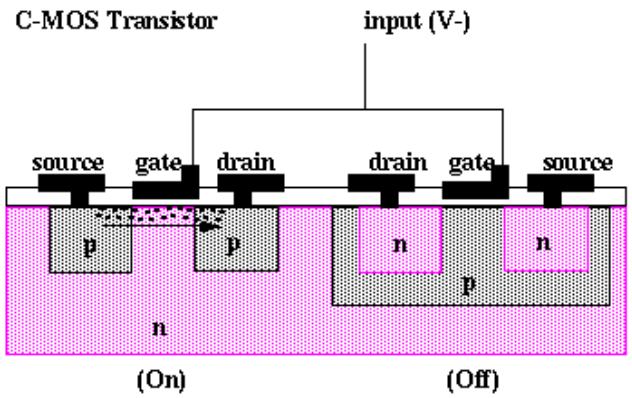
$W' = W/\alpha$

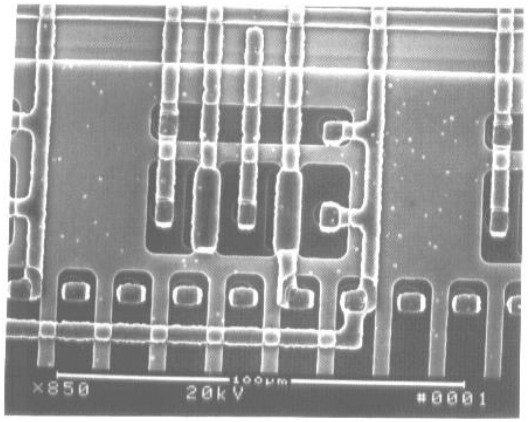
$L' = L/\alpha$

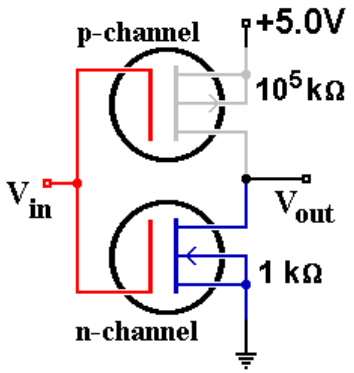
$D' = D/\alpha$



Aplicaciones: Circuitos Lógicos
Tecnología CMOS

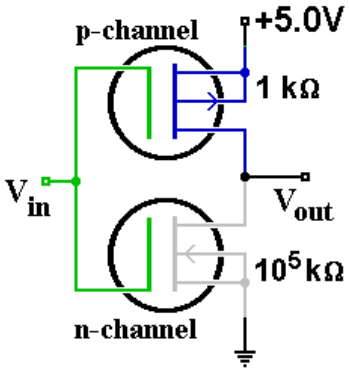






CMOS
invertor

in: HI
on: n-channel
off: p-channel
out: LO



CMOS
invertor

in: LO
on: p-channel
off: n-channel
out: HI

Inversor (NOT)

Aplicaciones: Memorias RAM

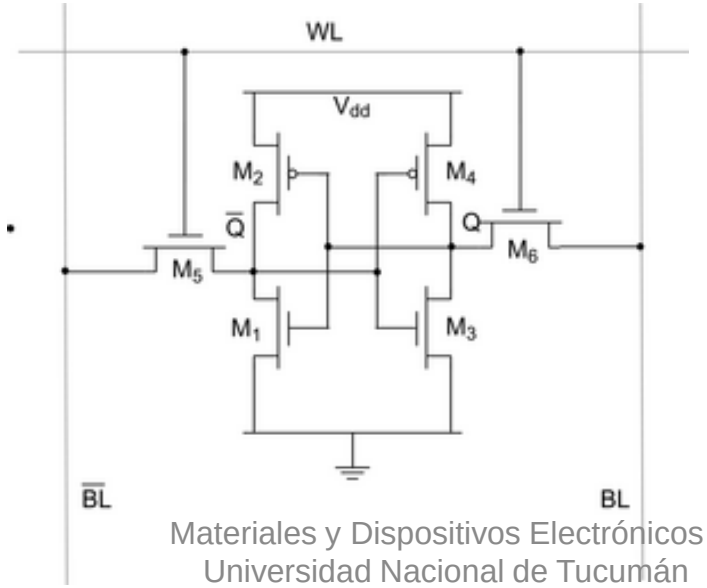
DRAM

Se almacena un “1” en la celda cargando el condensador mediante una V_G en fila y V_D en bit

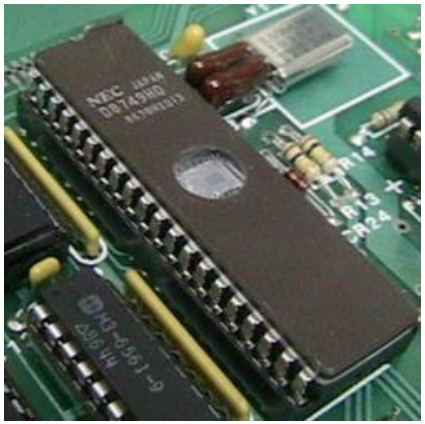
La lectura se hace aplicando V_G en fila y midiendo la corriente en la línea bit

La lectura es un proceso destructivo. Hay que restaurar el valor leído

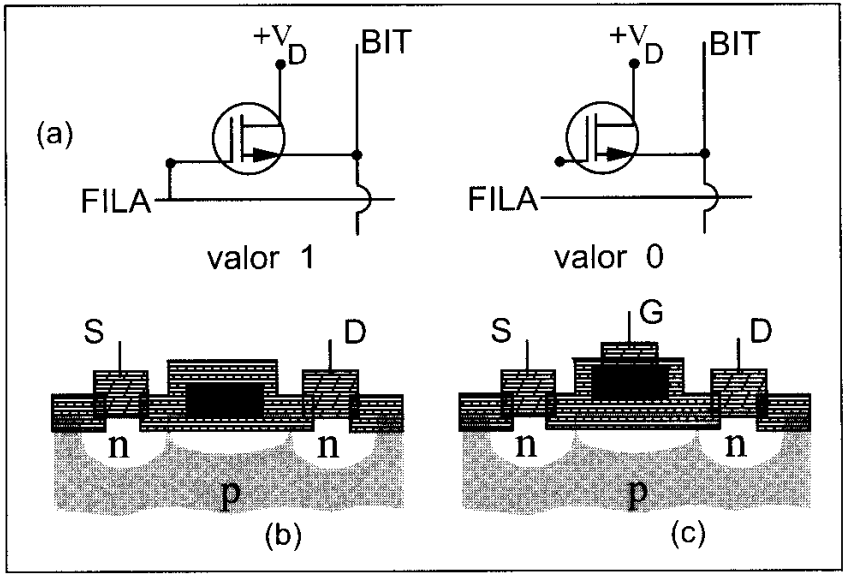
SRAM



Aplicaciones: Memorias ROM

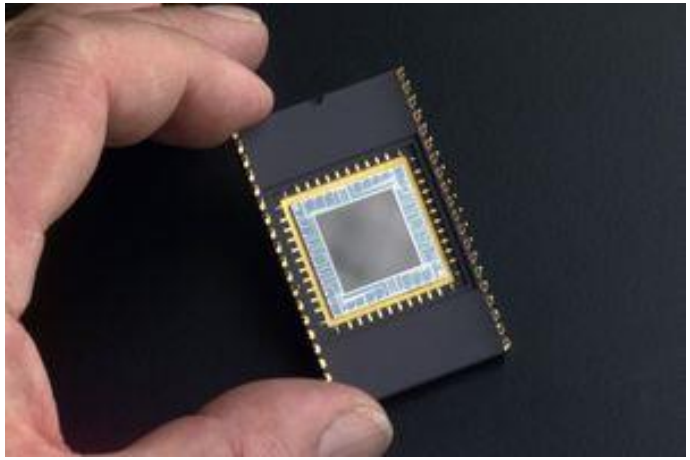


EPROM

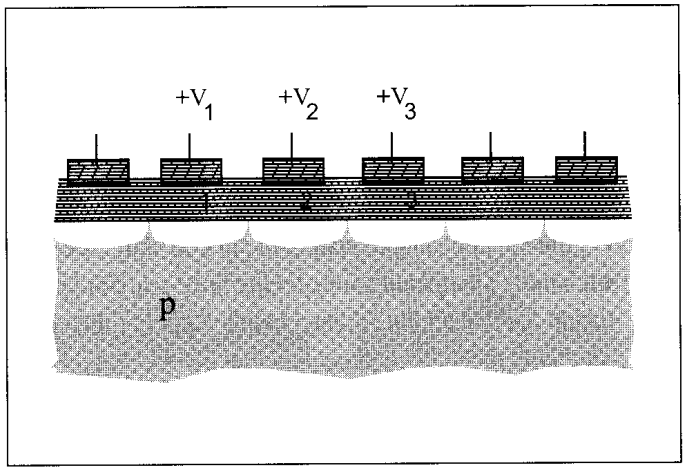


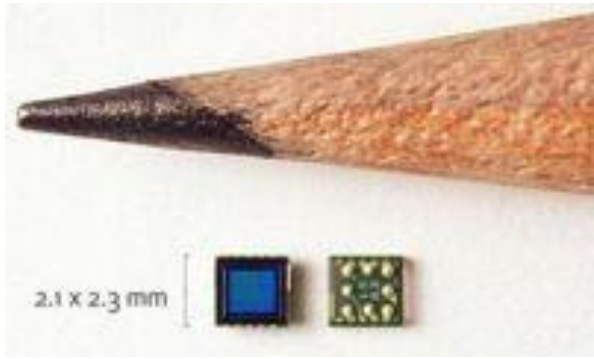
MOSFET ROM

Aplicaciones: CCD



CCD





CMOS sensor