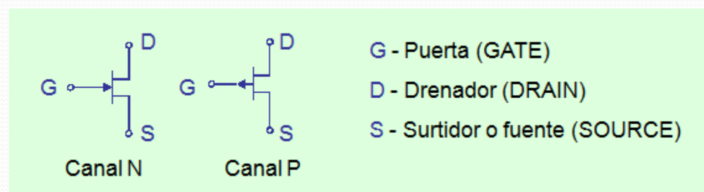
Transistores Efecto de Campo JFET

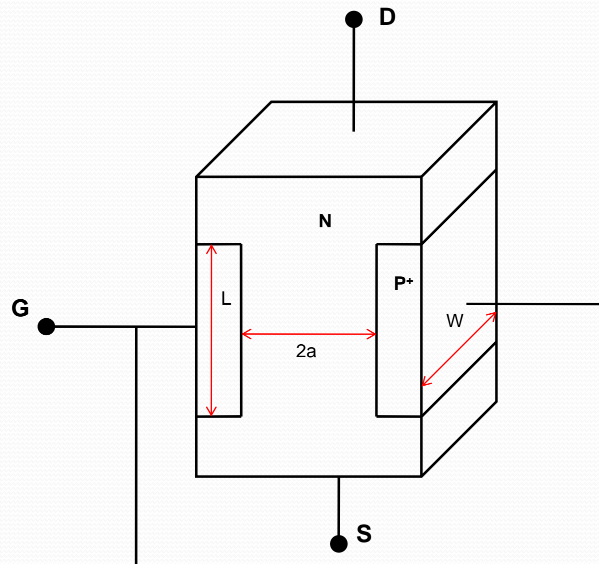
Definición

- JFET=Transistor de Efecto de Campo de Juntura
- Es un dispositivo de 3 terminales: Drenador-Fuente-Compuerta
- Transistor Unipolar (Un solo tipo de corriente-electrones o huecos)
- Corriente I_{DS} controlada por V_{GS}

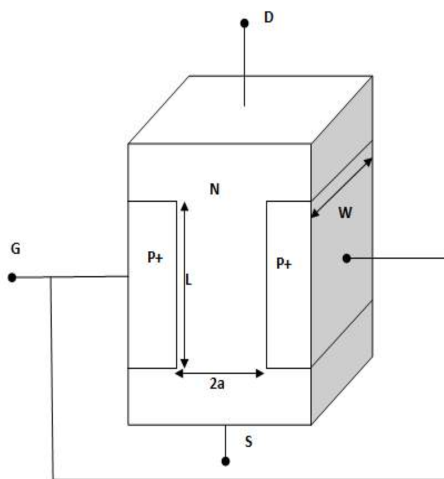
Símbolo circuital



Estructura del JFET

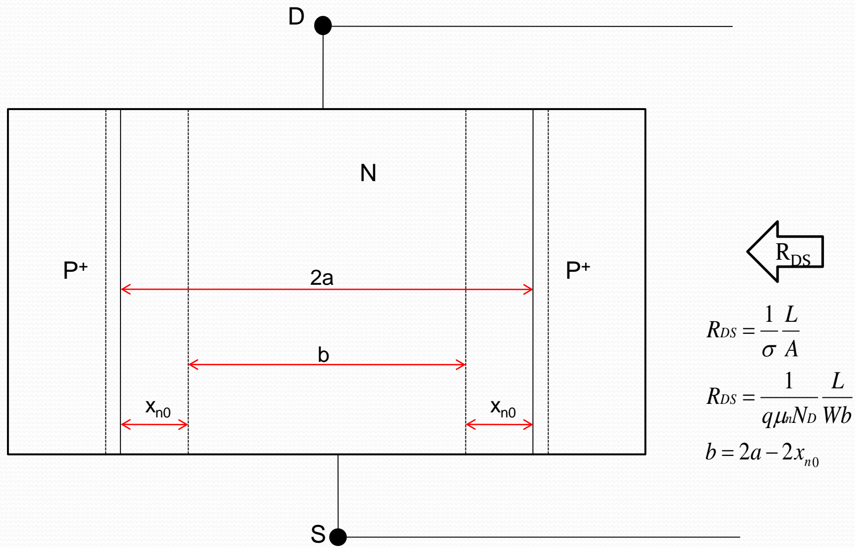


Estructura (JFET Canal N)

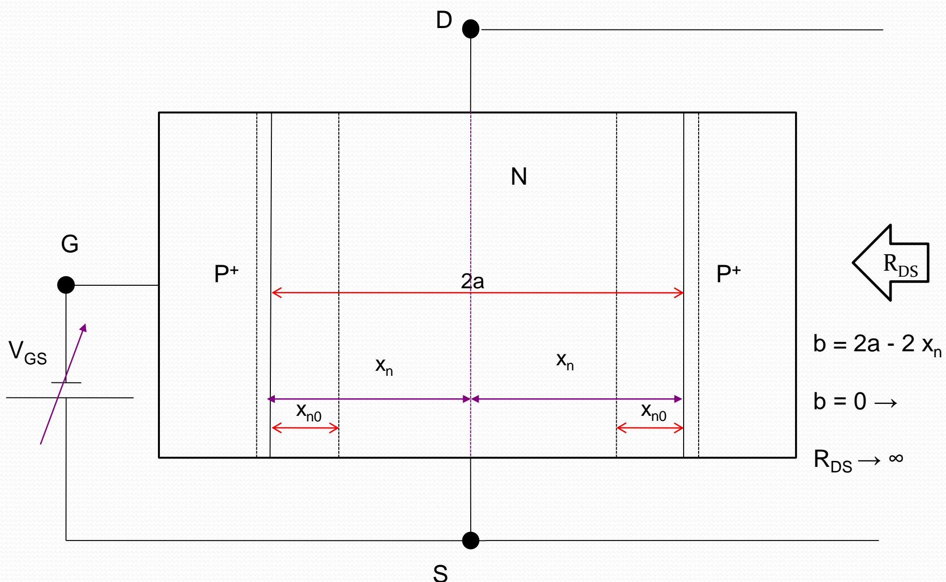


W: Profundidad del Canal
L: Largo del Canal
2a: Ancho Metalúrgico del Canal
N_D: Concentración Zona N canal
N_A: Concentración Zona P Compuertas
$N_A >> N_D \Rightarrow P^+N$

Principio de Funcionamiento (1)



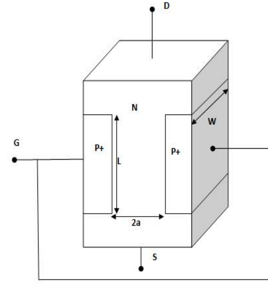
Principio de Funcionamiento (2)



Cuando b = 0 no existe canal y $R_{DS} \rightarrow \infty$

La tensión V_{GS} para la que b = 0 se define como TENSION DE ESTRANGULAMIENTO (V_P)

V_P es un parámetro del dispositivo
Depende de la fabricación



$$x_n = \left[\frac{2\varepsilon}{qN_D}\frac{1}{\left(1+\frac{N_D}{N_A}\right)}\right]^{\frac{1}{2}} * [V_{jo} - V_{GS}]^{\frac{1}{2}} \qquad x_n \approx \left[\frac{2\varepsilon}{qN_D}\right]^{\frac{1}{2}} * [V_{jo} - V_{GS}]^{\frac{1}{2}}$$

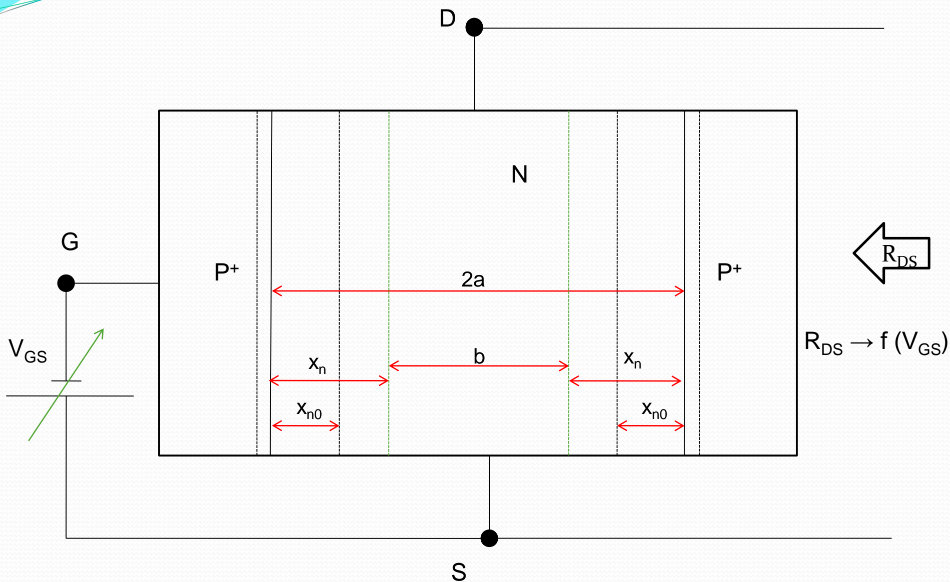
$$x_n \approx K_1 * [V_{jo} - V_{GS}]^{\frac{1}{2}} \qquad K_1 = \left[\frac{2\varepsilon}{qN_D}\right]^{\frac{1}{2}} \qquad K_1 \rightarrow \text{Constante que depende de la Fabricación}$$

$$a = K_1 (V_{jo} + V_P)^{\frac{1}{2}} \quad \text{suponiendo } V_{jo} \langle\langle V_P \qquad a = K_1 (V_P)^{\frac{1}{2}} \quad \Rightarrow V_P = \left(\frac{a}{K_1}\right)^2$$

$$V_P = a^2 \frac{qN_D}{2\varepsilon}$$

7

Principio de Funcionamiento (3)



Dispositivos Electrónicos-FACET

8

$$R_{DS} = \frac{1}{\sigma}\frac{L}{A} \qquad R_{DS} = \frac{1}{q\,\mu_n\,N_D}\frac{L}{W.b} \qquad b = 2a - 2x_n$$

$$x_n = \left[\frac{2\varepsilon}{qN_D}\frac{1}{\left(1+\frac{N_D}{N_A}\right)}\right]^{\frac{1}{2}} * [V_{jo} - V_{GS}]^{\frac{1}{2}} \qquad x_n \approx \left[\frac{2\varepsilon}{qN_D}\right]^{\frac{1}{2}} * [V_{jo} - V_{GS}]^{\frac{1}{2}}$$

$$x_n \approx K_1 * [V_{jo} - V_{GS}]^{\frac{1}{2}} \qquad K_1 = \left[\frac{2\varepsilon}{qN_D}\right]^{\frac{1}{2}}$$

$K_1 \rightarrow$ Constante que depende de la Fabricación

$$b = 2\left[a - K_1 (V_{jo} - V_{GS})\right]^{\frac{1}{2}} \qquad b = 2a\left[1 - \frac{K_1}{a}(V_{jo} - V_{GS})^{\frac{1}{2}}\right]$$

$$b = 2a\left[1 - \left(\frac{V_{jo} - V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] \qquad V_{jo} \langle\langle V_{GS} \qquad b = 2a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$$

$$b \rightarrow f(V_{GS}) \Rightarrow R_{DS} \rightarrow f(V_{GS})$$

$$R_{DS} = \frac{L}{q\mu_n N_D W 2a}\frac{1}{\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]}$$

$$V_{GS} = V_p \rightarrow R_{DS} \rightarrow \infty$$

$$V_{GS} = 0 \rightarrow R_{DS} = R_{DSON}$$

$$R_{DSON} = \frac{L}{2aq\mu_n N_D W} \rightarrow$$

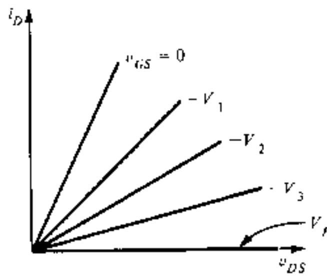
R_{DSON} es un parámetro del dispositivo y depende de la fabricación

$$R_{DS} = R_{DSON}\frac{1}{\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]}$$

$$I_{DS} = \frac{V_{DS}}{R_{DS}} \rightarrow I_{DS} = \frac{1}{R_{DSON}}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] V_{DS}$$

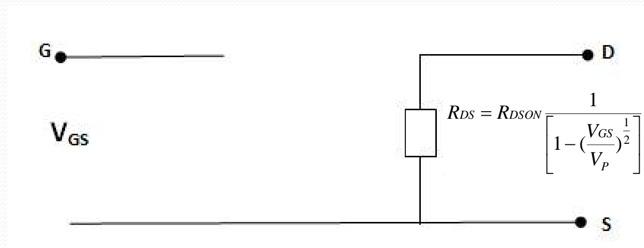
Relación V-I del JFET para $V_{DS} \approx 0$

CARACTERISTICA V-I PARA ZONA OHMICA

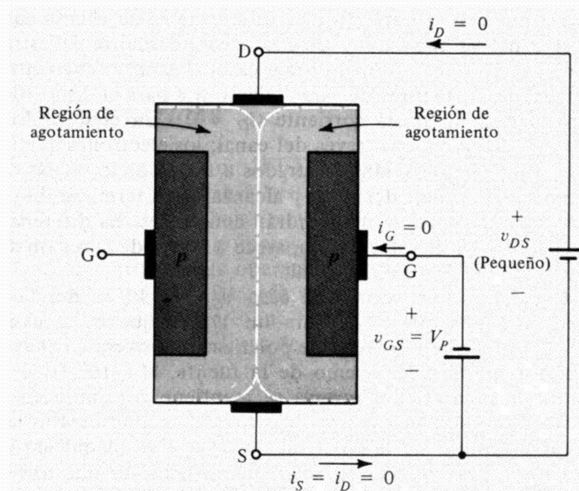


La tensión Vgs controla la geometría del canal : Este control provoca la variación del área del resistor entre drenador y fuente.

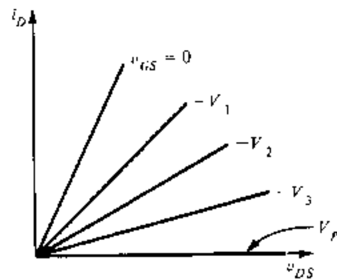
Resistencia Drenador-Fuente->f(V_{GS})

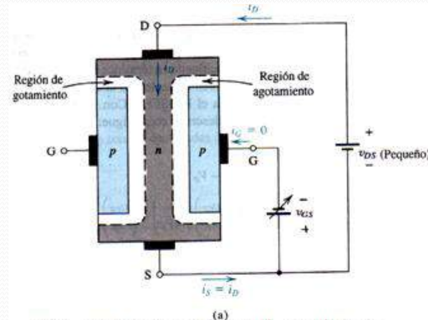


- Cuando $V_{GS} = V_P$ la zona de transición de la juntura P-N invade toda la región N, impidiéndose totalmente la conducción.
- (**Corte del canal**)



Zona Óhmica (Control de Compuerta)

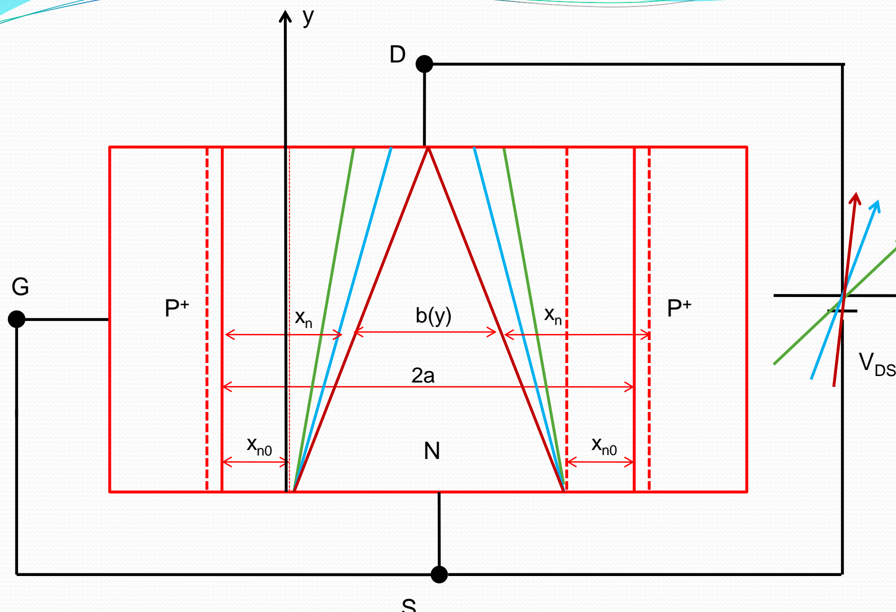




•En esta región el canal conductor entre drenador y fuente **se comporta como una resistencia R_{DS}**

•La R_{DS} va aumentando a medida que se estrecha el canal, a consecuencia de la polarización inversa producida por V_{GS}

Principio de Funcionamiento (4)



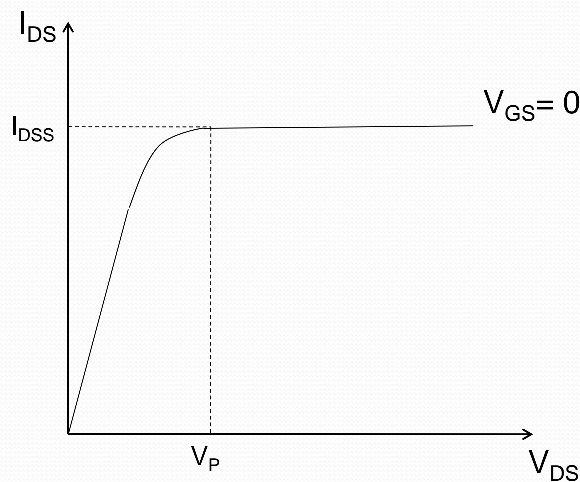
- VDS comienza a aumentar hasta alcanzar el valor de Vp.
- En ese punto, el canal se estrangula en la zona de drenador.
- Cuando se estrangula, IDS no puede aumentar más y alcanza su máximo valor I_{DSS}
- I_{DSS} Corriente D-S con $V_{GS} = 0$ y $V_{DS} \geq V_P$
- I_{DSS} es un parámetro del dispositivo.

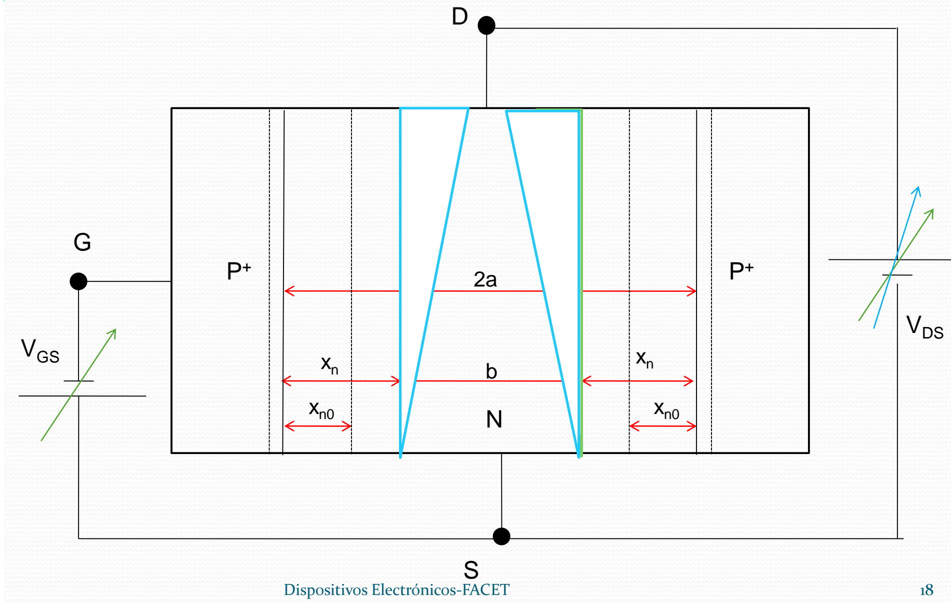
$$J_{DS}(y) = \sigma E_{DS}(y) \qquad J_{DS}(y) = \frac{I_{DS}}{b(y) \times W}$$

Cuando $V_{DS}\uparrow$ b(y)$\downarrow \Rightarrow J_{DS}\uparrow$ y para mantener la igualdad E(y)$\uparrow$

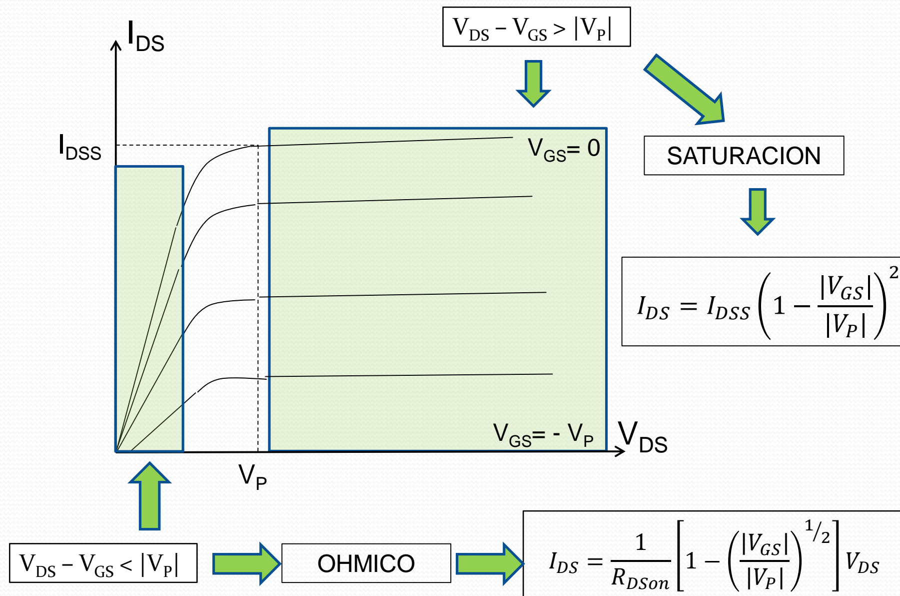
• Como J_{DS} (y) ↑ es tan grande E(y) crece hasta alcanzar el valor para el cual se deja de cumplir la ley de Ohm.
• La velocidad de deriva vd satura y la movilidad deja de ser constante.
• vd = μ E

CARACTERISTICA V- I PARA V_{GS} = 0



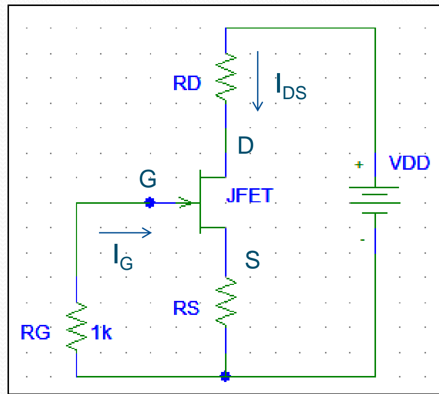


Principio de Funcionamiento (5)
D
G
P+
2a
P+
VDS
VGS
xn
b
xn
xn0
N
xn0
S
Dispositivos Electrónicos-FACET
18



CARACTERISTICA V- I
IDS
VDS – VGS > |VP|
IDSS
VGS= 0
SATURACION
$I_{DS} = I_{DSS}\left(1 - \frac{|V_{GS}|}{|V_P|}\right)^2$
VGS= - VP
VDS
VP
VDS – VGS < |VP|
OHMICO
$I_{DS} = \frac{1}{R_{DSon}}\left[1 - \left(\frac{|V_{GS}|}{|V_P|}\right)^{1/2}\right]V_{DS}$

POLARIZACION DEL JFET



$V_{DS} - V_{GS} > |V_P|$ → SATURACION

$$V_{DS} = V_{DD} - I_{DS} \times R_S - I_{DS} \times R_D$$

$$V_{GS} + I_{DS} \times R_S + I_G \times R_G = 0$$

$$I_G \approx 0 \Rightarrow I_G \times R_G = 0 \qquad V_{GS} = -I_{DS} \times R_S$$

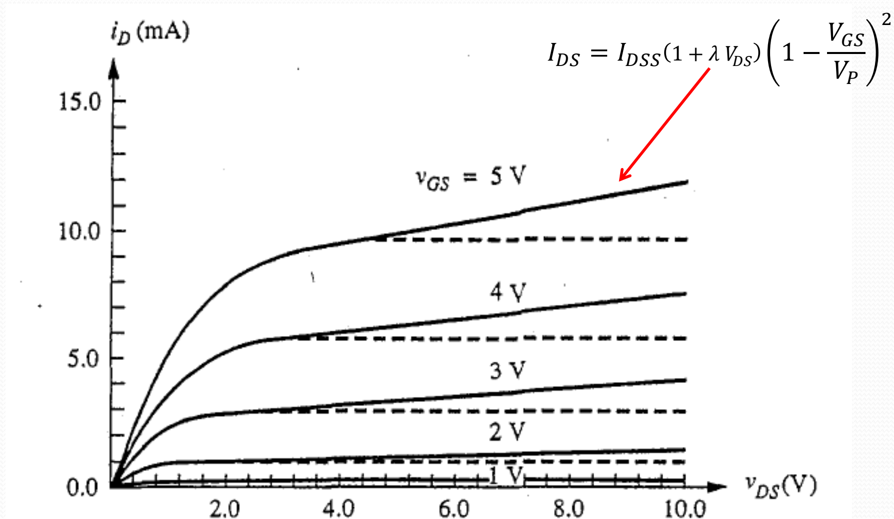
$$V_{DS} - V_{GS} = V_{DD} - I_{DS} \times R_D > V_P$$

$$R_D < \frac{V_{DD} - V_P}{I_{DS}} \rightarrow Para\ saturacion$$

$$0 \leq I_{DS} \leq I_{DSS} \rightarrow Rango\ de\ I_{DS}$$

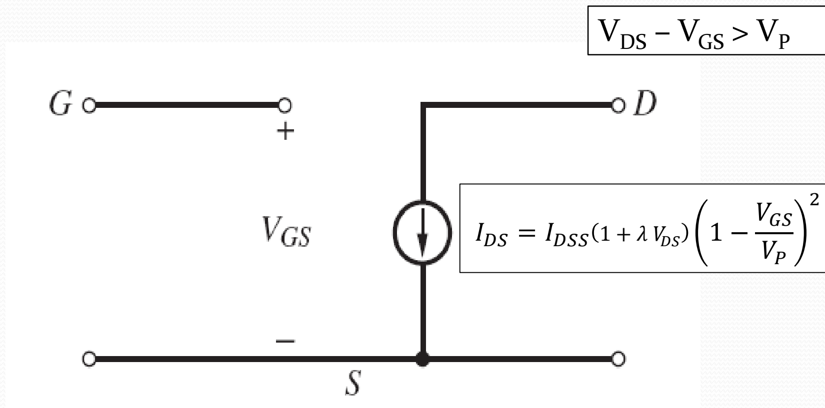
$$V_P \leq V_{DD} \leq V_{DSMAX} \rightarrow Rango\ de\ V_{DD}$$

Modulación del Largo del Canal



Modelo del JFET en zona de saturación

$$V_{DS} - V_{GS} > V_P$$



Dispositivos Electrónicos

23

Si el JFET esta polarizado en SATURACION

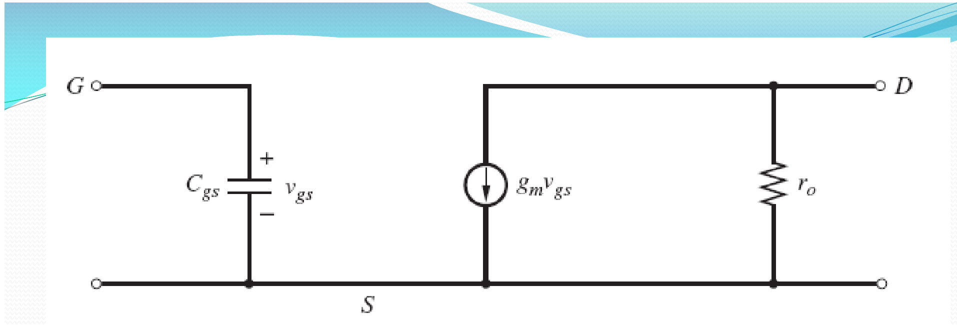
$$I_{DS} = I_{DSS}(1 + \lambda V_{DS})\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$g_m = \frac{dI_{DS}}{dV_{GS}}\bigg|_{\overline{Q}} \qquad r_0 = \frac{dV_{DS}}{dI_{DS}}\bigg|_{\overline{Q}}$$

En el punto de polarización (Q)

$$V_{GS} = V_{GSP} \qquad I_{DS} = I_{DSP} \qquad V_{DS} = V_{DSP}$$

24



$$g_m = -\frac{2\,I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)\Bigg|_Q \qquad r_0 = \frac{1}{\lambda\, I_{DSP}}\Bigg|_Q$$

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 + \dfrac{V_{GS}}{V_{j0}}}}$$

VCR2N/4N/7N
Vishay Siliconix

JFET Voltage-Controlled Resistors

PRODUCT SUMMARY			
Part Number	$V_{GS(off)}$ Max (V)	$V_{(BR)GSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)
VCR2N	–7	–25	60
VCR4N	–7	–25	600
VCR7N	–5	–25	8000

FEATURES
- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance

BENEFITS
- Gain Ranging Capability/Wide Range Signal Attenuation
- No Circuit Interaction
- Simplified Drive

APPLICATIONS
- Variable Gain Amplifiers
- Voltage Controlled Oscillator
- AGC

DESCRIPTION

The VCR2N/4N/7N JFET voltage controlled resistors have an ac drain-source resistance that is controlled by a dc bias voltage (V_{GS}) applied to their high impedance gate terminal. Minimum r_{DS} occurs when V_{GS} = 0 V. As V_{GS} approaches the pinch-off voltage, r_{DS} rapidly increases. This series of junction FETs is intended for applications where the drain-source voltage is a low-level ac signal with no dc component.

Key to device performance is the predictable r_{DS} change versus V_{GS} bias where:

$$r_{DS}\text{bias} \approx \frac{r_{DS}(@\,V_{GS}=0)}{1 - \left|\frac{V_{GS}}{V_{GS(off)}}\right|}$$

These n-channel devices feature $r_{DS(on)}$ ranging from 20 to 8000 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500 (see Military Information).

VCR2N/4N/7N

Vishay Siliconix

ABSOLUTE MAXIMUM RATINGS[a]

Gate-Source, Gate-Drain Voltage .... –25 V
Gate Current .... 10 mA
Power Dissipation[b] .... 300 mW
Operating Junction Temperature Range .... –55 to 175° C
Storage Temperature .... –65 to 200° C

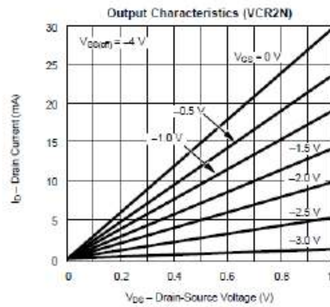
Lead Temperature ($^1/_{16}$" from case for 10 sec.) .... 300° C

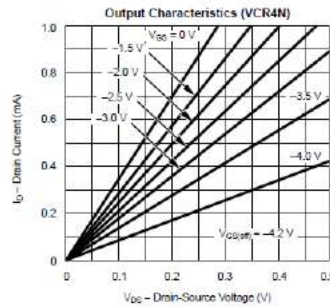
Notes:
a. T_A = 25°C unless otherwise noted.
b. Derate 2 mW/°C above 25°C.

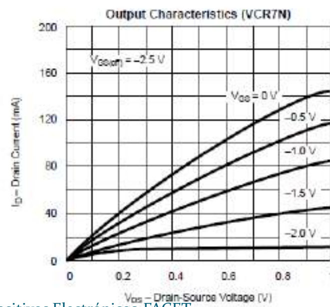
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Typ[a]	Limits						Unit
				VCR2N		VCR4N		VCR7N		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 µA, V_{DS} = 0 V	–55	–25		–25		–25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 µA		–3.5	–7	–3.5	–7	–2.5	–5	V
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V			–5		–0.2		–0.1	nA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, I_D = 10 mA		20	60					Ω
		V_{GS} = 0 V, I_D = 1 mA				200	600			Ω
		V_{GS} = 0 V, I_D = 0.1 mA						4000	8000	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7							V
Dynamic										
Drain-Source On-Resistance	$r_{ds(on)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz		20	60	200	600	4000	8000	Ω
Drain-Gate Capacitance	C_{dg}	V_{GD} = –10 V, I_S = 0 mA, f = 1 MHz			7.5		3		1.5	pF
Source-Gate Capacitance	C_{sg}	V_{GS} = –10 V, I_D = 0 mA, f = 1 kHz			7.5		3		1.5	pF

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)







TO-206AA (TO-18)

S, D, G and Case

Top View

VCR2N, VCR4N

TO-206AF (TO-72)

S, C, D, G

Top View

VCR7N

APPLICATIONS

A simple application of a FET VCR is shown in Figure 1, the circuit for a voltage divider attenuator.

R, V_{IN}, V_{OUT}, V_{GS}, VCR

FIGURE 1. Simple Attenuator Circuit

The output voltage is:

$$V_{OUT} = \frac{V_{IN}\, r_{DS}}{R + r_{DS}}$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which V_{OUT} can assume is:

$$V_{OUT(min)} = \frac{V_{IN}\, r_{DS(on)}}{R + r_{DS(on)}}$$

Since r_{DS} can be extremely large, the highest value is:

$$V_{OUT(max)} = V_{IN}$$

NXP Semiconductors **Product specification**

N-channel junction FET BF862

FEATURES

- High transition frequency for excellent sensitivity in AM car radios
- High transfer admittance.

APPLICATIONS

- Pre-amplifiers in AM car radios.

DESCRIPTION

Silicon N-channel symmetrical junction field-effect transistor in a SOT23 package. Drain and source are interchangeable.

PINNING SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

2, 1, 3, g, d, s

Top view

MAM036

Marking code: 2Ap.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	20	V
V_{GSoff}	gate-source cut-off voltage		−0.3	−0.8	−1.2	V
I_{DSS}	drain-source current		10	–	25	mA
P_{tot}	total power dissipation	$T_s \leq 90$ °C	–	–	300	mW
$\lvert y_{fs} \rvert$	transfer admittance		35	45	–	mS
T_j	junction temperature		–	–	150	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
V_{DG}	drain-gate voltage		–	20	V
V_{GS}	gate-source voltage		–	−20	V
I_{DS}	drain-source current		–	40	mA
I_G	forward gate current		–	10	mA
P_{tot}	total power dissipation	$T_s \leq 90$ °C; note 1	–	300	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	200	K/W

Note

1. Soldering point of the gate lead.

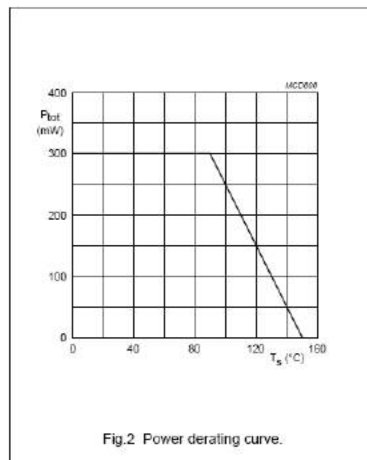


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_{GS} = −1 μA; V_{DS} = 0	−20	−	−	V
V_{GS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	−	−	1	V
V_{GSoff}	gate-source cut-off voltage	V_{DS} = 8 V; I_D = 1 μA	−0.3	−0.8	−1.2	V
I_{GSS}	reverse gate current	V_{GS} = −15 V; V_{DS} = 0	−	−	−1	nA
I_{DSS}	drain-source current	V_{GS} = 0; V_{DS} = 8 V	10	−	25	mA

DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{GS} = 0; V_{DS} = 8 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	common source forward transfer admittance	T_j = 25 °C	35	45	−	mS
g_{os}	common source output conductance	T_j = 25 °C	−	180	400	μS
C_{iss}	input capacitance	f = 1 MHz	−	10	−	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	−	1.9	−	pF
e_n	equivalent noise input voltage	f = 100 kHz	−	0.8	−	nV/√Hz
f_T	transition frequency		−	715	−	MHz

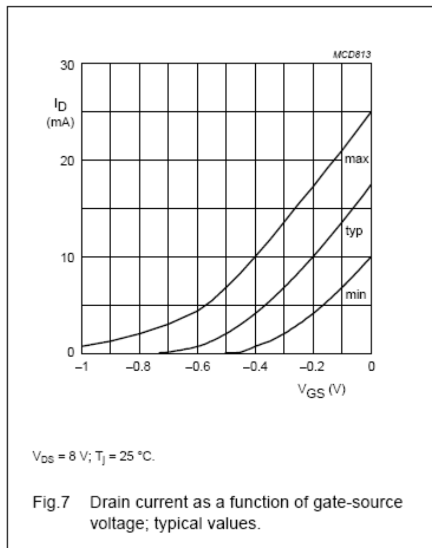


Fig.7 Drain current as a function of gate-source voltage; typical values.

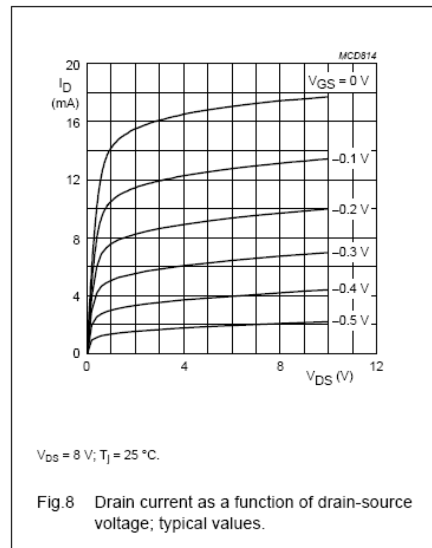


Fig.8 Drain current as a function of drain-source voltage; typical values.